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EFFECTS OF EVAPORATED TELLURIUM BACK BUFFER LAYER ON CdTe SOLAR CELL

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The heavily doped tellurium (Te) -rich layer is an effective back contact material by chemical etching CdTe traditionally. But the reported studies drew the conflicting conclusions concerning the physical mechanisms about Te layer in CdTe. In this paper an evaporated Te layer based on a $CuCl_2$ treated CdTe surface was developed for application in CdS/CdT[1]e solar cells, and the effects of the evaporated Te buffer on the device performance were evaluated in detail. It is found that the effects of Te layer on the device performance depend on the CdTe surface. As a result, an open circuit voltage up to 825mV and filling factor up to 70% was obtained for the devices with an evaporated Te buffer after $CuCl_2$ treatment.

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1. Introduction

CdTe solar cells are one of the most promising solar cells with an appropriate band gap (1.45eV) and high absorption coefficient (>10^4cm^{-1}) currently, and the highest conversion efficiency of 22.1% with open voltage (V_{oc}) of 887.2mV has been achieved [1]. Nevertheless, forming an ohmic back contact remains one of the most challenging and meaningful barriers to the production of efficient, long-life CdTe thin-film solar cells. Typically, tunneling contact is achieved to overcome this problem, one way is adding a heavily doped p-type semiconductor material including ZnTe: Cu [2, 3] or Cu_xTe [4-6] between CdTe and the metal electrode, and the other way is creating a heavily doped tellurium-rich CdTe surface, such as chemical etching CdTe with bromine-methanol [7] or nitric-phosphoric acid solution [8].

Due to the vacuum incompatibility of the chemical etching method, researchers tried to prepare tellurium by vacuum compatible method. Xia et al. prepared Te/Cu back contact by sputtering method, and achieved an efficiency of 14.1% [9]. Colorado state university (CSU) incorporated tellurium into the whole CdTe device by evaporation method, and achieved a high conversion efficiency of 18.3% [10]. It is shown that evaporated tellurium is a promising back contact material, and it is essential to study the role of tellurium in CdTe solar cells.

However, the previous studies drew the conflicting conclusions concerning the physical mechanisms about the using of Te layer in CdTe. Tyan proposed that tellurium by evaporation was not suitable for low-resistance contact [11]. Kraft and Fritsche also deemed that there was a valence band offset (VBO) of 0.4 ~ 0.6 eV between CdTe and Te interface, forming a blocking Schottky barrier that was not suitable for low resistance back contact, and speculated that etching led to a tunneling contact [12, 13]. The opposite point of view was proposed by Song and Moore et al. Song and Moore of CSU showed that tellurium layer could inhibit forward current, reduce the degree of valence band bending, reduce the voltage drop and improve the V_{oc} by simulation [14, 15]. Therefore, it is necessary to further elucidate the effects of evaporated Te back buffer on CdTe solar cells.

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In this work, we applied an evaporated tellurium back buffer to CdTe solar cells and studied the effects of tellurium both on undoped CdTe surface and on the highly doped CdTe surface by dark J-V, bias QE and J-V-T test techniques experimentally. We have found that the effect of evaporated Te buffer could be beneficial or harmful which depends on CdTe surface states.

2. Experimental

2.1. Device fabrication

We have prepared different CdTe solar cells to study the effects of Te on the CdTe solar cells. In order to investigate the effect of Te on the undoped CdTe surface and on the highly doped CdTe surface, we prepared CdTe solar cells with two basic structures: FTO/CdS/CdTe/Te(w/o)/Au and FTO/CdS/CdTe ($CuCl_2$ treatment)/Te(w/o)/Au. The reason why $CuCl_2$ is chosen as a Cu source is that $CuCl_2$ solution has been studied to provide a more stable doping effect with a small amount of Cu while CuCl is easy to oxidize and deteriorate due to the unstable +1 valence Cu ion [16]. Besides, we explored the effect of Te with different thickness on CdTe solar cells with following structures: FTO/CdS/CdTe ($CuCl_2$ treatment)/Te (0, 10, 30, 50nm)/Au. The Schematic diagram of the structure of polycrystalline CdTe thin film solar cells is shown in Fig. 1.

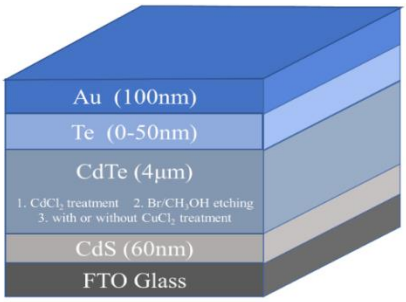

Fig. 1. Schematic diagram of the structure of CdTe thin film solar cells.

In our experiments, FTO substrates are Tec-15 provided by Pilkington, which were cleaned with Amway glass cleaner first, then ultrasonic cleaning and boiling several times. CdS layer was fabricated with ~ 60 nm by chemical bath deposition, then a ~ 4 μm CdTe layer was deposited by self-designed vapor transport deposition under Ar-O_2 atmosphere with substrate temperature of 450℃[17, 18]. This was followed by a wet $CdCl_2$ treatment containing an ultrasonic spray with 0.1mol/L $CdCl_2$ aqueous solution at 150°C for 2min and a post annealing treatment at 390℃for 35 min in an air (N_2:O_2−4:1) ambient. After that, the samples were etched in a 2‰ Br/CH_3OH solution for 4 seconds to remove surface oxides. Next Te films with different thicknesses were deposited on some CdTe films with and without $CuCl_2$ treatment by Electron beam evaporation with a velocity at 0.02 ~ 0.03 nm/s. Here $CuCl_2$ treatment is as follows: at first the samples were dipped in 150 mg/L $CuCl_2$ aqueous solution for 20 s; then the samples were dried at 60 ℃for 15 min in air ambient; at last the samples were annealed in tube furnace at 220 ℃for 15 min in an air (N_2:O_2=4:1) ambient. More details of the $CuCl_2$ treatment could be found elsewhere [19]. After Te deposition, there is no post-heat treatment. Finally, a 100nm Au layer was deposited as electrode. All cells were defined by laser scribing into ~16 individual cells with the area of 0.0707 cm^2 or 0.24 cm^2.

2.2 Film and device characterization

The Te thin film electrical properties were measured in van der Pauw method through a Hall effect system with a set of a Keithley 7065 Hall effect card, 6485 picoammeter, 2182A nanovoltmeter, and 6220 constant current source. The work function of the Te thin film was

obtained from Kelvin Probe Force Microscopy (KPFM, Bruker Nano Inc DI Multimode 8), and the work function of the probe was calibrated by Au films. The current density-voltage (J-V) characteristics of the devices were measured using a pulsed light solar simulator under AM1.5 at 100 mW·cm^2 irradiation. The light intensity was calibrated with a GaAs standard cell (PV Measurements, Inc). Bias quantum efficiency (QE) was measured by QEX10 (PV Measurements, Inc.) at AC mode and performed under nonstandard conditions (voltage bias), named as apparent quantum efficiency (AQE), which was calibrated with a Si standard cell. The dark J-V curves were measured with an Agilent 4284A precision LCR meter in the air. The capacitance-voltage (C-V) characteristics were measured at a frequency of 1 MHz in the dark with Agilent 4284A precision LCR meter. Above all of the measurements were performed at room temperature. The J-V-T measurements were performed in dark with DC voltage sweeping from -0.5 to 1.2 V. The temperature was varied from 298 K to 338 K with increments of 5 K. The device was heated by a homemade resistive heater and the temperature of device was controlled individually by an adhesive thermocouple (ST-50, PKC, Inc.)

3. Results and discussion

3.1. The electrical and electronic properties of Te thin films

Hall measurements show that Te thin film deposited on plain glass is p-type, and the resistivity, sheet resistance, carrier density and hall mobility are $0.26\,\Omega\cdot\mathrm{cm}$, $1.41\times10^4\,\Omega/\mathrm{square}$, $2.65\times10^{18}\,\mathrm{cm}^{-3}$ and $8.99\,\mathrm{cm}^2/V\cdot S$, respectively. The magnitude of the resistivity, sheet resistance and carrier density are consistent with previous publications [14, 20]. It is worth noting that the carrier mobility we measured is slightly higher than the reported result (~3.3 $\mathrm{cm}^2/V\cdot S$) [21], which is helpful to the carriers transport.

The work function of the Te buffer layer was gained from the surface contact potential difference (CPD) between tip and sample by KPFM at room temperature [22]. According to the CPD between the tip and the sample as shown in Fig. 2(a), the work function of the tip and the Te film are 4.95 eV and 5.10 eV, respectively. We derived the Fermi level from the Boltzmann approximation for the concentration of holes [23], which is shown below:

$$p = N_{\mathrm{V}}\exp[-{(E_{\mathrm{V}}-E_{\mathrm{F}})}/{K_{\mathrm{B}}T}] \tag{1}$$

Where N_{V} is the effective density of states in the valence band, E_{V} is the valence band level, K_{B} is Boltzmann constant, p is the hole density and T is the temperature. According to the effective mass of holes, reported at 0.45 m_{e} [24], where m_{e} is the mass of an electron, the effective density of states in the Te valence band (N_{V}) is calculated and has a value of $7.6\times10^{18}cm^{-3}$. According to Eq. (1), This will place E_{F} approximately ~0.03eV from E_{V} for carrier densities measured with Hall techniques (~$2.65\times10^{18}cm^{-3}$).

Thus, the Fermi energy level of tellurium is 0.03 eV above the valence band, and the VBO between CdTe and Te layer is ~ 0.62 eV. Combined with the band gap of Te reported at 0.33eV [20], we drew a simple Te band diagram as shown in Fig. 2(b).

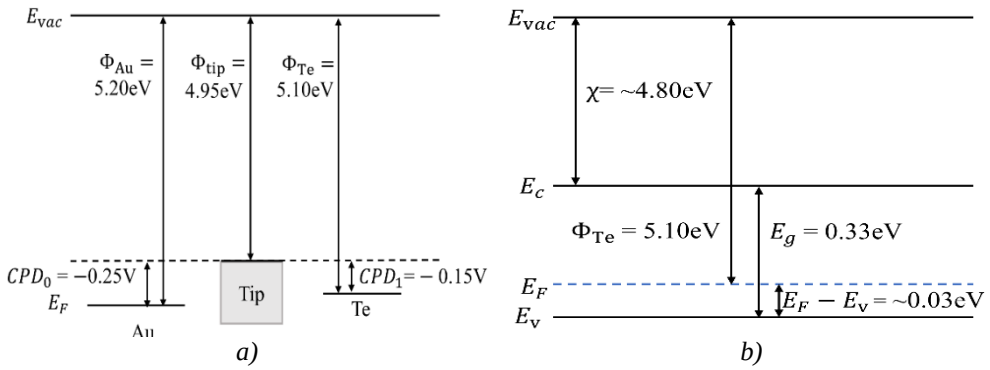

Fig. 2. (a) Band alignment diagram showing E_F of Au and Te samples relative to the AFM tip, and absolute Φ values for them. (b) Schematic band diagram of Te with band gap (E_g), the position of Fermi level (E_F) and electron affinity (χ) labeled (not to scale).

3.2. Effects of Te on CdTe solar cells with and without $CuCl_2$ treatment

Box charts of device performances for each type of samples are shown in Fig. 3. "0" means as-deposited devices and "Te" means devices with only 30nm tellurium. "$CuCl_2$" means devices with $CuCl_2$ treatment without tellurium while "$CuCl_2$+Te" represents devices with both $CuCl_2$ treatment and tellurium deposition. The efficiency (E_{ff}) of the devices with 30nm Te is about 10%, which is similar with that of as-deposited devices. After tellurium deposition, the decrease in the V_{oc} is more than 50 mV, from 794 to 740 mV, which is mainly attributed to a large VBO value of ~0.62eV as shown in Fig. 4(a). There is a Schottky barrier at the interface between CdTe and Te, which is confirmed by Kraft et al. [12]. The Schottky barrier at the back contact is demonstrated to some extent by dark J-V and bias QE measurements that will be discussed later. For the devices with 30nm tellurium, the series resistance (R_s) is decreased and the fill factor (*FF*) is improved, which is resulting from that Te atoms diffused into CdTe surface and formed Te-related acceptor defects, improving CdTe surface carrier density [25], facilitating holes tunneling. However, the weak effect of tunneling was compromised with the effect of the large Schottky barrier, so the device efficiency almost unchanged. Therefore, the performance of the devices with a Te back buffer is similar with that of the as-deposited device performance.

The efficiency of $CuCl_2$ treated devices increases obviously to about 12%, and the improvement on efficiency is mainly ascribed to the increase in the V_{oc} from 793 to 817 mV and the increase in the *FF* from about 61% to 68 % as shown in Fig. 3 and Fig. 5(a). After $CuCl_2$ treatment, some Cu^{2+} ions diffused into CdTe layer and formed Cu related shallow acceptor states [16, 26], which increased the bulk hole density of CdTe. Increasing the hole density can improve the V_{oc} of CdTe solar cells, which has already been reported to be one of the most efficient strategies [27, 28]. Meanwhile, a strong p-type back surface is formed, the reason is not only that many Cu ions are concentrated close to the back-contact surface but also that highly degenerated p+ copper telluride (Cu_xTe) is easy to form in the presence of Te and Cu^{2+} after heat treatment. The *FF* of $CuCl_2$ treated devices increases to more than 66%, which is primarily related with the decrease of R_s. All in all, the efficiency of the device with $CuCl_2$ treatment is improved.

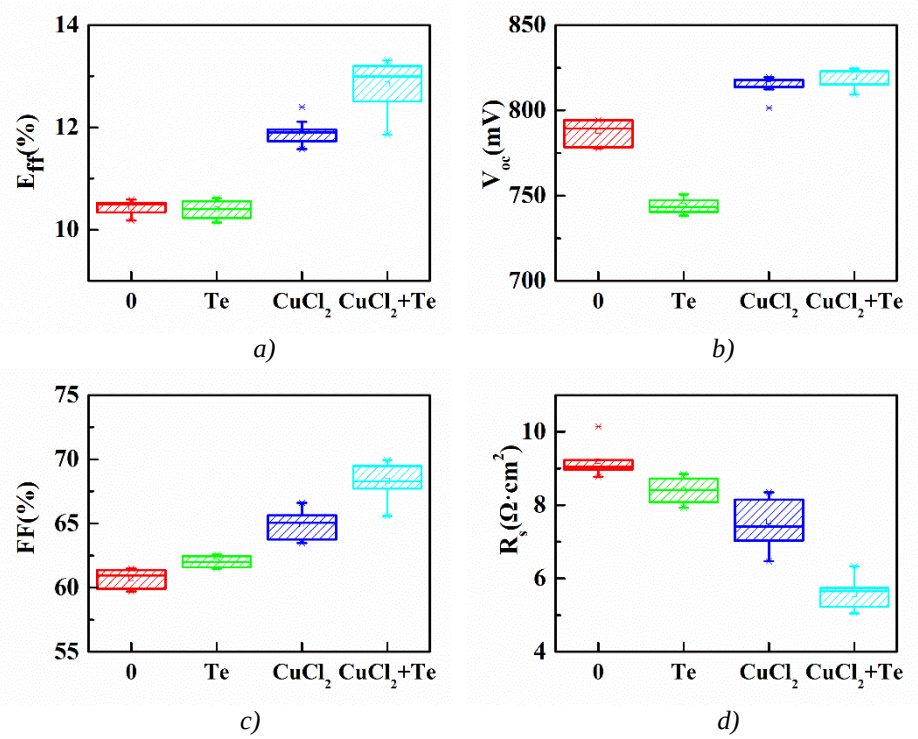

Fig. 3. The box charts of parameters for CdTe devices with different back contact structures.

While, the device efficiency greatly is further improved by introducing a Te layer after $CuCl_2$ treatment, mainly resulting from the enhancement of *FF*. The improved performance is arising from the decrease of R_S. The C-V curves of the CdTe devices were shown in Fig. 6(b) and the carrier density of CdTe layer was calculated. The carrier density of $CuCl_2$+Te devices with a value of 5.98×10^{13} cm^{-3} is larger than that of $CuCl_2$ devices with a value of 3.95×10^{13} cm^{-3}. Thus, a narrower barrier is formed at the Cu doped p+ CdTe surface and p-type Te back buffer interface as shown in Fig. 4(b). A narrower barrier facilitates hole tunneling forming an ohmic contact. Except for additional Te layer, $CuCl_2$ and $CuCl_2$+Te devices have the same preparation process, so it is reasonable to consider that the increase of carrier density is due to Te atoms' diffusion into CdTe layer. This also confirms the previous speculation that Te atoms diffuse into CdTe surface layer for the devices with 30nm Te deposition, therefore *FF* improves.

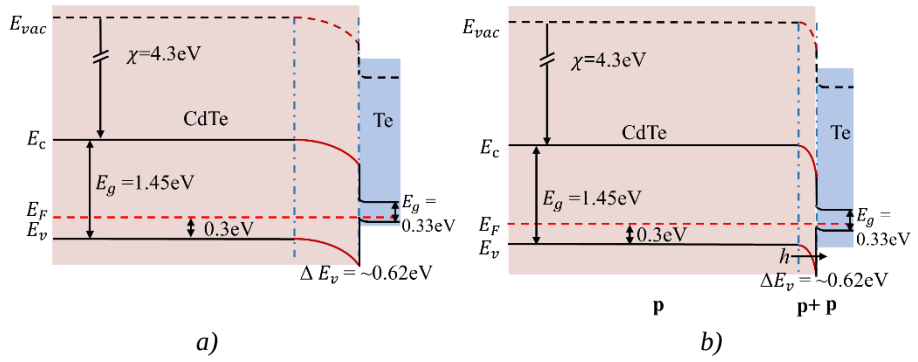

Fig. 4. Schematic energy band structure of CdTe and Te layers, (a) CdTe without $CuCl_2$ treatment, (b) CdTe with $CuCl_2$ treatment.

The dark J-V and AQE of CdTe solar cells with different back contacts are shown in Fig. 5. As shown in Fig. 5(b), the devices only with a Te back buffer present a larger rollover than the as-deposited device, which is attributed to the presence of a higher barrier at the back contact [12]. $CuCl_2$ treated devices present a reduced rollover, furthermore, the rollover was nearly eliminated when a Te back buffer was introduced after $CuCl_2$ treatment, this is in accordance with bias (V_{bias}=V_{oc}+ 100 mV) QE shown in Fig. 5(c). The bias QE can qualitatively determine the back barrier height [29]. The as-deposited device with reverse QE response from the CdTe region suggests a higher back barrier than those $CuCl_2$ treated devices. The devices with $CuCl_2$ treatment have a smaller reverse peak at around 830 nm suggesting a lower back barrier. It is worth noting that $CuCl_2$+Te devices have almost no negative peaks in the CdTe region, indicating that there is almost no back barrier. Therefore, V_{oc} and *FF* for the CdTe solar cells were enhanced greatly due to the band modification of tellurium in the CdTe/Te interface with $CuCl_2$ treatment.

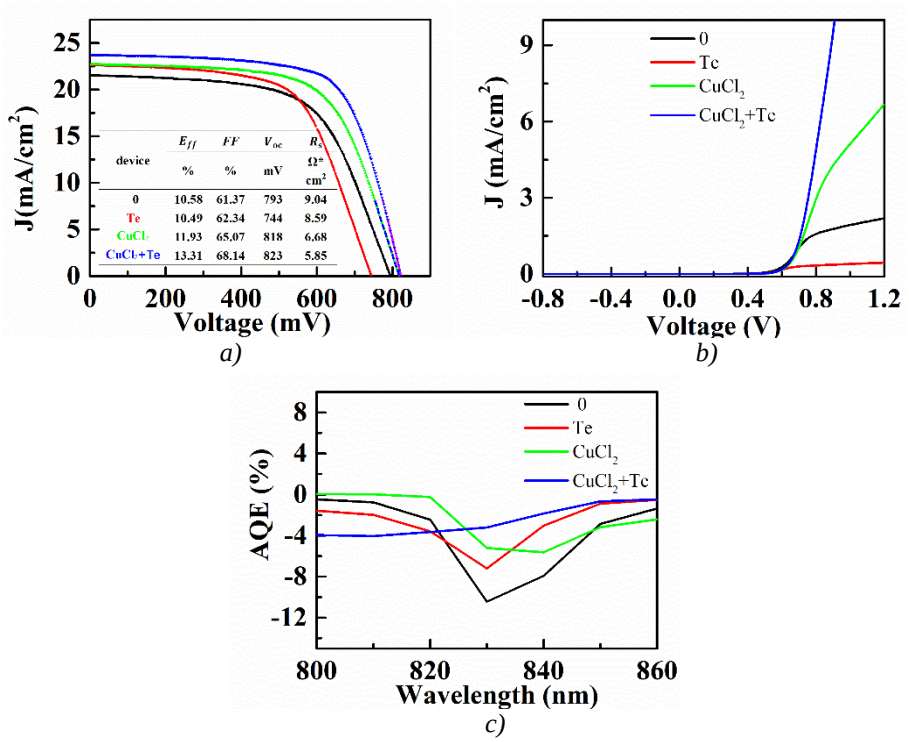

Fig. 5. (a) Light J-V, (b) dark J-V and (c) bias (V_{bias} = V_{oc} + 100 mV) QE at 800nm-860nm for various CdTe solar cells.

J-V-T measurements were carried out for CdTe solar cells with and without Te back buffer to calculate back contact barriers (qΦ) [30-32] and further understand the effects of Te back buffer. We use "turning current" J_0, which is the current at the transition from the positive Log(J)-V curvature to the negative curvature not shown here, to drew the Arrhenius point of $\ln(J_0/T^2)$ verse $1/K_BT$, in order to further extract the activation energy (E_a) for the back barrier shown in Fig. 6(a). The height of back barrier is measured to be 0.593 eV for the devices with Te film, which is why such devices have a low V_{oc}. It is significantly reduced to 0.388eV for the devices with $CuCl_2$ treatment, partially responsible for the improvement of *FF* and V_{oc}. The height of back contact barrier is further reduced and has a minimum value of 0.367eV after introducing a Te back buffer. This indicates that introducing a Te back buffer after $CuCl_2$ treatment can further reduce back contact barrier.

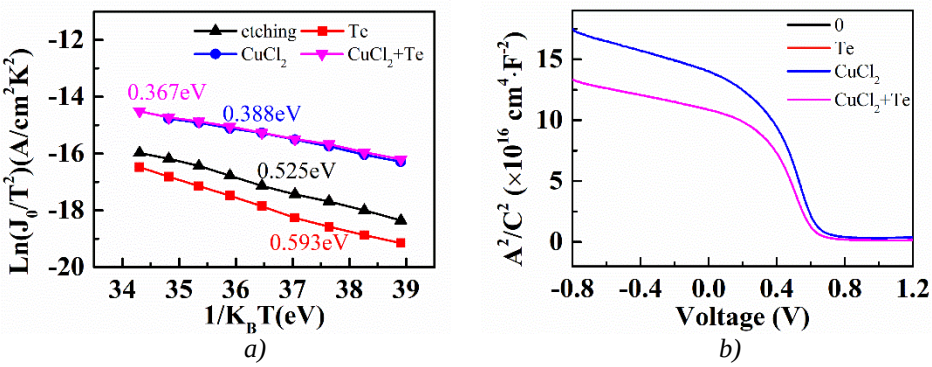

Fig. 6. (a) Dark J-V-T curves of the various CdTe devices to calculate back contact barriers (qΦ), (b) C-V curve of CdTe devices.

3.3. Effects of Te with different thickness on the CdTe solar cells

The effects of different Te thicknesses on the device performance were explored. We fabricated CdTe solar cells with 10, 30, 50nm tellurium and no tellurium deposition as a reference, they all have $CuCl_2$ treatment. The box charts of these devices with different Te thicknesses are shown in Fig. 7.

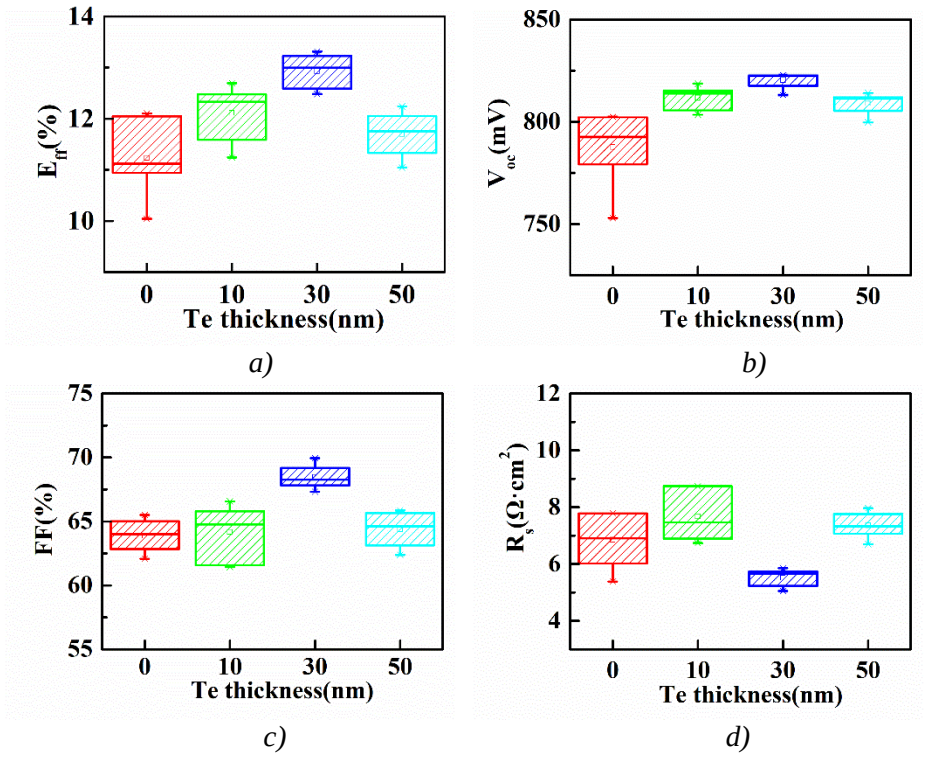

Fig. 7. The box charts of CdTe solar cells with $CuCl_2$ and 0, 10, 30 and 50 nm Te.

The light J-V curves of best device are shown in Fig. 8(a). The performances of all the devices with tellurium become better than that without tellurium regardless of tellurium thickness, which is attributed to the improvement of V_{oc} and *FF*. The devices with 30nm tellurium are better than that with 0, 10nm and 50nm tellurium. The poor performance of 10nm tellurium devices may result from that too thin tellurium film could not cover CdTe surface completely so that lacking of enough material to realize the bulk properties of the tellurium [21]. The poor efficiency of the device with 50nm tellurium is related with higher series resistance of thick tellurium.

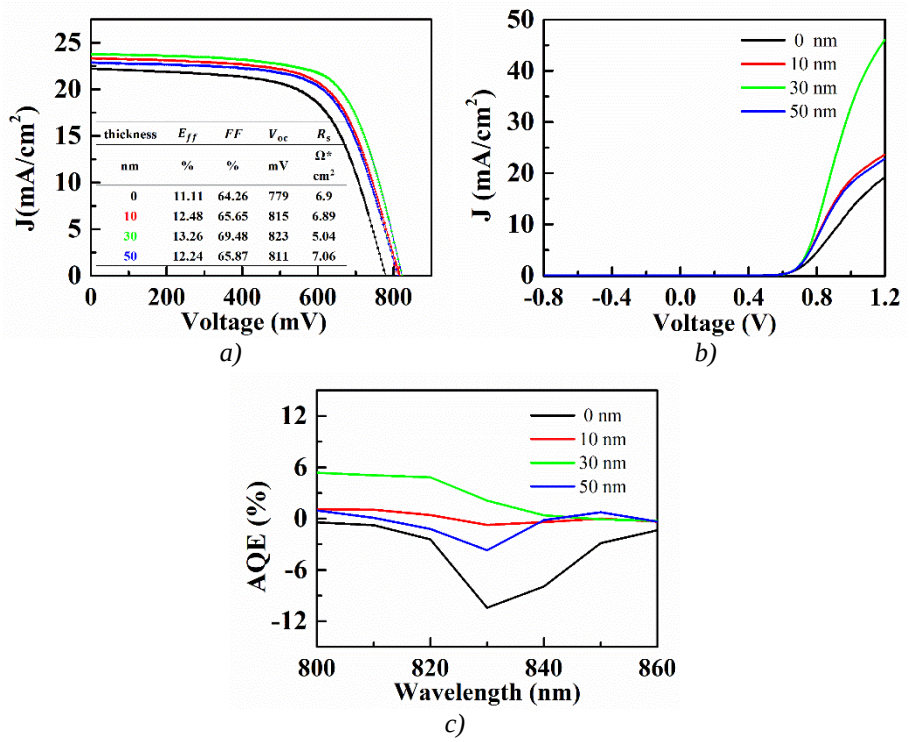

Fig. 8. (a) Light J-V, (b) dark J-V and (c) bias (V_{bias} = V_{oc} + 100 mV) QE at 800nm-860nm for CdTe solar cells with $CuCl_2$ and 0, 10, 30 and 50 nm Te.

The dark J-V and AQE of CdTe solar cells with $CuCl_2$ and 0, 10, 30 and 50 nm Te are shown in Fig. 8. As shown in Fig. 8(b), The device without tellurium presented a larger rollover than the other devices, which is attributed to the presence of the higher barrier at the back contact. The devices with 10nm and 50nm Te thicknesses presented a reduced rollover. It was nearly eliminated when a 30 nm tellurium was introduced after $CuCl_2$ treatment. Fig. 8(c) shows bias (V_{bias} = V_{oc} + 100 mV) QE of typical devices, and related parameters are summarized in Fig. 8(a). The devices with 30nm Te thicknesses show almost no reverse QE response from the CdTe region, which suggests an eliminated back barrier. The devices with 50nm tellurium and without tellurium had a tiny reverse peak at around 830 nm suggesting a lower back barrier. Therefore, the optimal performance of the device was achieved by introducing a 30nm Te back buffer on the CdTe solar cells with $CuCl_2$ treatment.

4. Conclusions

We have prepared solar cells with evaporated Te back buffer and studied the effects of evaporated Te layer in CdS/CdTe solar cells in details. The back barrier of the devices only with a Te back buffer is higher due to the larger CdTe/Te interface VBO around 0.62 eV, which resulted in barriers for hole transport to the Au electrode. Therefore, an evaporated tellurium was not suitable as low resistance back contact for CdTe solar cells without $CuCl_2$ treatment or without heavy doping. The back barrier was significantly reduced for the CdTe devices by introducing a 30nm Te back buffer after $CuCl_2$ treatment, so series resistance is decreased and *FF* of the devices is improved, thus improving the conversion efficiency of CdS/CdTe solar cells. The improved performance is primarily attributed to the narrower barrier zone of p-type Te back buffer and $CuCl_2$ treated p+ CdTe interface. In summary, evaporated tellurium thin film is a good option for back contact of CdTe solar cells, whereas doped CdTe back surface with Cu or other elements is necessary.

Acknowledgements

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References

[1] M. A. Green, Y. Hishikawa, W. Warta, E. D. Dunlop, D. H. Levi, J. Hohl-Ebinger, A. W. Y. Ho-Baillie, Progress. Photovolt. Res. Appl. **25** (7), 668 (2017).
[2] J. Li, D. R. Diercks, T. R. Ohno, C. W. Warren, M. C. Lonergan, J. D. Beach, C. A. Wolden, Sol. Energy. Mater. Sol. Cells **133**, 208 (2015).
[3] C. A. Wolden, A. Abbas, J. Li, D. R. Diercks, D. M. Meysing, T. R. Ohno, J. D. Beach, T. M. Barnes, J. M. Walls, Sol. Energy. Mater. Sol. Cells **147**, 203 (2016).
[4] B. Späth, K. Lakus-Wollny, J. Fritsche, C. S. Ferekides, A. Klein, W. Jaegermann, Thin Solid Films **515**(15), 6172 (2007).
[5] A. Bosio, R. Ciprian, A. Lamperti, I. Rago, B. Ressel, G. Rosa, M. Stupar, E. Weschke, Sol. Energy **176**, (2018).
[6] J. Zhou, X. Wu, A. Duda, G. Teeter, S.H. Demtsu, Thin Solid Films **515**(18), 7364 (2007).
[7] I. M. Kotina, L. M. Tukhkonen, G. V. Patsekina, A. V. Shchukarev, G. M. Gusinskii, Semicond. Sci. Technol. **13**(8), 890 (1998).
[8] X. Li, D. W. Niles, F. S. Hasoon, R. J. Matson, P. Sheldon, J. Vac. Sci. Technol. A **17**(3), 805 (1999).
[9] W. Xia, H. Lin, H. N. Wu, C. W. Tang, I. Irfan, C. Wang, Y. Gao, Sol. Energy. Mater. Sol. Cells **128**, 411 (2014).
[10] A. H. Munshi, J. M. Kephart, A. Abbas, T. M. Shimpi, K. L. Barth, J. M. Walls, W. S. Sampath, Sol. Energy. Mater. Sol. Cells **176**, 9 (2018).
[11] Author, Semiconductor devices having improved low-resistance contacts to p-type CdTe, and method of preparation, U.S, No. 4319069, (1982).
[12] D. Kraft, A. Thißen, M. Campo, M. Beerbom, T. Mayer, A. Klein, W. Jaegermann, Mat. Res. Soc. Symp. Proc. **668**, H7.5.1 (2001).
[13] J. Fritsche, D. Kraft, A. Thißen, T. Mayer, A. Klein, W. Jaegermann, Thin Solid Films, **403-404**, 252 (2002).
[14] A. Moore, T. Song, J. Sites, MRS Advances **2**(53), 3195 (2017).
[15] T. Song, A. Moore, J. R. Sites, IEEE J. Photovolt, **8**(1), 293 (2018).
[16] E. Artegiani, D. Menossi, H. Shiel, V. Dhanak, J. D. Major, A. Gasparotto, K. Sun, A. Romeo, Progress. Photovolt. Res. Appl. **27**(8), 706 (2019).
[17] S. Cao, L. Wu, L. Feng, W. Wang, J. Zhang, X. Yu, X. Li, W. Li, B. Li, J. Inorg. Mater. **31**(2), 141 (2016).
[18] H. Gu, A. Ren, J. Zhang, K. Li, C. Li, W. Wang, H. Xu, J. Mater Sci: Mater in Electron. **28**(13), 9442 (2017).
[19] T. Wang, S. Du, W. Li, C. Liu, J. Zhang, L. Wu, B. Li, G. Zeng, Mater. Sci. Semicond. Process **72**, 46 (2017).
[20] A. Goswami, S.M. Ojha, Thin Solid Films **16**(2), 187 (1973).
[21] A. Moore, Performance and metastability of CdTe solar cells with a Te back contact buffer layer, PH.D. dissertation, Colorado State University, (2017).
[22] J. Loos, Adv. Mater. **17**(15), 1821 (2005).
[23] S. M. Sze, K. K. Ng, Physics of Semiconductor Devices, Wiley, Hoboken, (2006).
[24] R. S. Caldwell, H. Y. Fan, Phys. Rev. **14**(3), 664 (1959).
[25] J. M. Burst, S. B. Farrell, D. S. Albin, E. Colegrove, M. O. Reese, J. N. Duenow, D. Kuciauskas, W. K. Metzger, APL Materials **4**(11), 116102 (2016).
[26] D. Krasikov, I. Sankin, J. Mater. Chem. A **5**(7), 3503 (2017).
[27] J. Sites, J. Pan, Thin Solid Films **515**(15), 6099 (2007).
[28] A. Kanevce, T. A. Gessert, IEEE J. Photovolt. **1**(1), 99 (2011).

[29] M. Gloeckler, J. R. Sites, J. Appl. Phys. **95**(8), 4438 (2004).
[30] G. Stollwerck, J. R. Sites, Proc. of the 13th Eu PVSEC, 2020 (1995).
[31] G. T. Koishiyev, J. R. Sites, S. S. Kulkarni, N. G. Dhere, Photovolt. Spec. Conf. 2008. 33rd IEEE, 1 (2008).
[32] A. Montgomery, L. Guo, C. Grice, R. A. Awni, S. Saurav, L. Li, Y. Yan, F. Yan, Progress. Photovolt. Res. Appl. **27**(8), 665 (2019).