MINIMIZED VOLTAGE DROP RECTIFIER CIRCUIT USING PIEZOELECTRIC TRANSDUCER FOR ENERGY HARVESTING

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Piezoelectric systems produce an AC voltage signal at the output and to utilize this voltage, It is required to convert this AC signal into DC with the assistance of the rectifying circuit. The aim of this research is to minimize the voltage drop V_D of the conventional diode by designing a diode circuit with the help of MOSFETS to be used in the rectifier. In conventional full bridge rectifier (Con-FBR) the power losses are very high because of diodes drop V_D. To minimize these losses the Con-FBR circuit is altered with the employment of both n-type and p-type MOSFETs to be operated in the deep triode (ohmic) region while blocking the reverse leakage which results in reducing the threshold voltage V_{TH} to few mV. Both positive and negative cycles are availed and investigated to extract the maximum output voltage. It is simulated in NI-Multisim (version 14.0) and is implemented using discrete components. The results show that the bridge rectifier using proposed low diode drop configuration has a better power conversion efficiency and can extract power '4' four times more than the Con-FBR.

1. Introduction

Energy harvesting is a process in which energy is derived from any other external source and capturing a small amount of energy that would otherwise be lost such as vibration, heat, light, and sound. The energy gained from the sources is then stored and converted into useable electrical energy [1]. Energy harvesting is achievable using different types of sources and these sources produce different amounts of power. A few of them are mentioned in Table 1.

Table 1. Power generation by different sources [3-4].

Energy source	Typical power
Solar light	100 m W/cm^2 (outdoor)
Thermoelectric	60 μ W/cm^2
Vibration	4 μ W/cm^3 (humanoid motion), 800 μ W/cm^3 (machines)
Ambient radio frequency	0.001 μ W/cm^2 (Wi-Fi)–0.1 μ W/cm^2 (GSM)
Acoustic noise	960 n W/cm^3
Ambient airflow	1 m W/cm^2

The energy harvesting is achievable by using different components as shown in Fig. 1. The first main component is the transducer or harvester which is the source of energy and converts

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it into electrical energy [4]. Different types of sources use a different type of conversion circuit as shown in Table 2.

Table 2. Power management circuits for different energy sources.

Ambient source	Transducers	Power management circuit
Light energy source	Solar devices	DC-DC converter
Mechanical energy source	Piezo-electric	AC-DC converter
Thermal energy source	Thermoelectric generators	Step-up DC-DC converter

After the conversion of energy, it is stored using batteries or capacitors and finally consumed by electronics circuits as shown in Fig. 1. There are a lot of advantages like it is environment-friendly, battery independent and etc. [1-5].
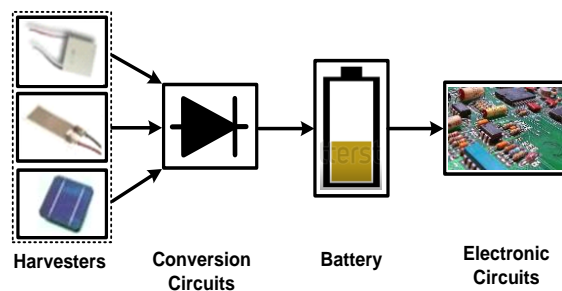

Harvesters   **Conversion Circuits**   **Battery**   **Electronic Circuits**

Fig. 1. Components of energy harvesting.

2. Piezoelectricity

The word piezo is derived from the Greek word "piezein" meaning press or squeeze. Piezoelectricity (PE) means producing electricity by means of pressure. The piezoelectric process (PEP) is the one in which electricity is produced by applying mechanical stress on it and the reverse process also exists in which stress is produced when an electric field (EF) is applied to it and is shown in Fig. 2 [6].
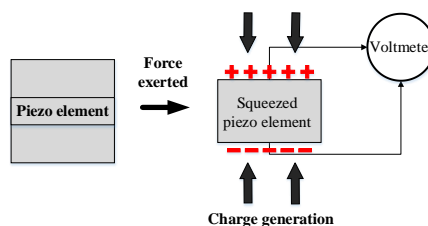

Fig. 2. Piezoelectric process (PEP) [6].

There are two processes of the PEP, which are Direct Piezoelectric Effect (DPE) and Reverse Piezoelectric Effect (RPE) as shown in Fig. 3(a) and 3(b). In DPE, the electric charges are created as a result of the mechanical stress like generators, sensors, switches, and etc., while in RPE, an electric field is applied to one of the faces of the crystal that undergoes mechanical distortion like actuators (for micro-positioning, micro-pumps, micro-valves), motors, and etc. [6].
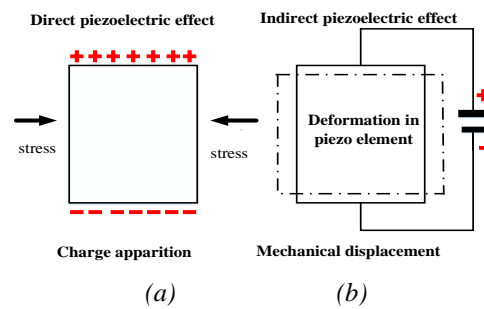
Fig. 3. (a) Direct piezoelectric effect (b) Reverse piezoelectric effect.

In the piezoelectric materials before the stress is applied to it there exists a center of symmetric for positive and negative charges. The center of gravity for negative and positive charges coincide with each other canceling each other and the net electrical output is zero. There are different types of PE materials as shown in Fig. 4. These materials have their own PE coefficients according to their different shapes. The details of these materials are mentioned in Table 3.

Table 2 Piezoelectric coefficients of different piezoelectric materials [6-9].

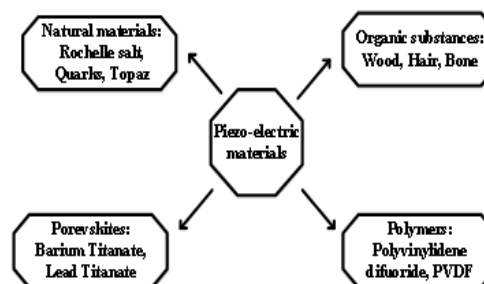| Materials	Shapes	Piezo-electric coefficient d_{31} (m/V or C/N)
Quarks	Single crystal	2.3
PZT	Sol-gel thin film	190 ~ 250
PVDF	Film	23
ZnO	Sputtered thin film	10.5 ~ 11.5
PZT	Sputtered thin film	100

Fig. 4. Types of Piezo-electric materials.

These materials have the following properties:

2.1. Anisotropic

The materials, whose properties are directional dependent are known as an isotropic material. Piezoelectric materials are anisotropic because their properties vary according to variation in the direction [8].

2.2. Non-Centro-symmetric

The materials show the reversible process by generation electric field when stress is applied to it and when it is subjected to the electric field, it generates strain changing its shape

slightly. That's why it is called a reversible process and these materials are widely used for both direct and indirect PE processes [8].

2.3. Reversible

Centro symmetric elements hold the inversion symmetry as one of its symmetry elements. A center of symmetry is a point through which the structure shows inversion symmetry as sown in Fig 5 (a). Mathematically, if there is an atom at Cartesian coordinates (x, y, z) relative to the center of symmetry, there must also be an atom at inverted Cartesian coordinates (-x, -y, -z) [8]. In the non-Centro-symmetric element, there is no inversion symmetry present in the element. Crystals having inversion symmetry cannot display the piezoelectric phenomenon as shown in Fig. 5 (b).

(a)   *(b)*

Fig. 5. (a) Centrosymmetric crystal having center of symmetry (b) Non-Centro-symmetric crystal having no center of symmetry [8].

The Working of PE Material can be explained by Fig. 6. When the material is placed under the stress by exerting force on it, the material shows the presence of the electric field. This phenomenon is known as piezoelectricity. Similarly, the reverse process also exists. In most of the crystals, the arrangement of the atoms is symmetrical but in the case of piezoelectric crystals such as quarks, the arrangement of the atoms is not symmetrical. On the whole piezoelectric crystals are electrically neutral because the atoms inside the crystal may not be symmetrically arranged, but their electrical charges are perfectly balanced with each other as positive charge in one place cancels out its nearby negative charge. When PE crystal is squeeze or stretch, the structure of a piezoelectric crystal is deformed pushing some of the atoms closer together or some of the atoms pushing apart from each other, the balance of positive and negative is upset, causing net electrical charges to appear. This effect carries through-out the whole structure of piezoelectric crystal, so net positive and negative charges appear on opposite faces of the piezoelectric crystals [9].
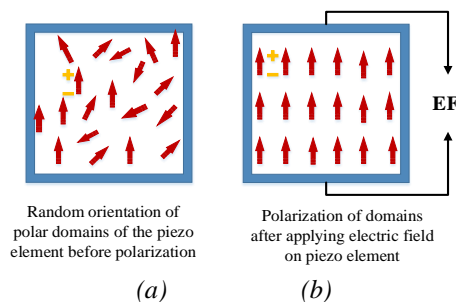

Random orientation of
polar domains of the piezo
element before polarization

Polarization of domains
after applying electric field
on piezo element

EF

(a)   *(b)*

Fig. 6. Polarization of piezoelectric crystals (a) Random orientation (b) Polarization domains

The following are the advantages and disadvantages of piezoelectric materials as shown in Table 3.

Table 3. Advantages and disadvantages of piezo-electric material [7-9].

Advantages	Disadvantages
No external energy source	Difficult to use
Output voltage ranges from (1-10) V	High frequency is needed
Highest energy density	More stress is needed

The first mathematical approach used for the piezoelectric effect was done on the base of its conversion ability from mechanical energy to electrical energy and vice versa. Curie brothers which show that the surface density of charges generated was proportional to the stress applied to the material [8].

$$P_p = dT \tag{1}$$

where P_d is the PE polarization which is proportional to the surface density of charges, d is the PE strain coefficient, T is the applied stress on the PE material. The eq: (1) was given for the DPE. Curie's brother also demonstrated the RPE and denoted it by

$$S_p = dE \tag{2}$$

where S_p is the strain produced by the PE effect, E is the magnitude of the applied electric field. It shows that the ratio between the strain produced and the magnitude of the applied electric field was equal [8-9]. The ratio of the direct phenomenon of the PE effect is equal to the reverse phenomenon of the piezoelectric effect. When we consider the elastic property of the material the direct and reverse phenomenon of piezo-electric material can be alternatively formulated. As, $T=cS$, so, eq: (1) becomes

$$P_p = dcS \tag{3}$$

If $dc = e$ (piezoelectric stress constant), then $P_P = eS$, then the above eq: (3) gives the relation between the polarization of PE material and the externally applied stress.

$$T_p = eE \tag{4}$$

Equation (4) shows that stress produced by the PE element is proportional to the externally applied electric field on it.

The PE effect also contributes to elastic constants because this PE phenomenon has the ability to causes an increase in the material's stiffness [9]. To understand this effect of PE material, the strain is applied to the PE material. This strain will have two effects. It will generate an elastic stress T_e which will be proportional to the mechanical strain and secondly, it will generate a piezoelectric polarization. Equation 5 shows the relation between the electric field and polarization of PE material. The electric field generated is proportional to the PE polarization generated due to the induced charges.

$$E_p = \frac{P_p}{\varepsilon} = \frac{eS}{\varepsilon} \tag{5}$$

where ε is the dielectric constant of the PE material. The total stress in the piezoelectric material will be

$$T = T_e + T_p$$

$$T = cS + \frac{e^2}{\varepsilon} S = \bar{c}S \qquad (6)$$

where, the constant= $\bar{c}$ is the PE stiffened constant, which causes an increase in the value of the elastic constant due to the piezoelectric effect [8, 9].

The Electrical model of PE transducers was proposed on the basis of its abilities. PE material converts the mechanical stress into electric current and vice versa generating charges. When it is attached to the circuit, charges will move and thus current is generated. So, PE transducers can be modeled using current sources. The electrodes attached to the PE transducers help in generating electric charges. The PE modules usually consist of a cantilever shaped substrate fixed at one side over which the piezoelectric sensor is placed. Piezoelectric transducer is sandwiched by monolithic electrode layers. The voltage being produced by piezoelectric transducers is very less. The output power decreases as the rectification circuits have their own voltage drops and power consumption. According to this design, the monolithic electrode layers are split into 'n' regions. When piezoelectric transducer vibrates, the voltage signals are generated and thus spreads into the n- regions all having the same amplitude, frequency, and phase [8-10].

The n-regions of the transducer can be connected in series as well as parallel. When the regions are connected in series, these results have increased the voltage by the factor n. However, when the n-regions are connected in parallel with each other, the voltage is the same as that of a monolithic piezoelectric transducer. Figure. 7(a) shows the equivalent circuit for the monolithic piezoelectric transducers and Fig. 7(b) shows the piezoelectric transducer which is split into 'n' regions.
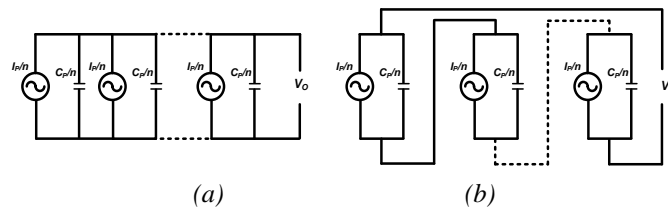

(a)   *(b)*

Fig. 7. (a) Circuitry of a monolithic piezoelectric transducer (b) n-region series connection of piezoelectric transducer.

The gaps present between the regions of the electrodes are assumed to be negligible. Therefore, the change in the vibration frequency and amplitude is also considered to be negligible. At first monolithic model of the piezoelectric transducer is analyzed in order to demonstrate the behavior of the n-region model of the piezoelectric transducer. When the transducer is under stress, the current and internal capacitance of the monolithic electric model is represented as I_p and C_p respectively. The current source is termed as $i_p(t)=I_p sin(\omega_p t)$ in parallel with the capacitor C_p and a resistor R_p. The I_p is the magnitude of the current and $\omega_p=2\pi f_p$, where f is the vibration frequency. The total charge produced in a half time period is given as

$$Q_{total} = \int_0^{T/2} I_o \sin(\omega t)dt = 2CV_{oc} \qquad (7)$$

In an open circuit, the overall generated charge Q_{total} flows through C_p. The open voltage amplitude for piezoelectric transduces is calculated as

$$V_{oc} = \frac{1}{2}\frac{Q_{total}}{C_p} = \frac{I_o}{\omega C_p} \qquad (8)$$

The output power consumed by a resistive load can be calculated by connecting a variable resistance R_L in parallel with the transducer. The load resistance R_L will have an impedance equal to the transducer, so it is varied until the same impedance is achieved. The amplitude of current passing through R_L can be given as

$$I_{R(j\omega)} = I_o \frac{Z_c}{Z_C + R_L} = \frac{I_o}{1 + j\omega R_L C_p} \tag{9}$$

The output power consumed can be calculated as

$$P_R = \frac{1}{2} | I_R^2 R_L | = \frac{I_o^2 / 2}{(1 / R_L) + \omega^2 C_p^2 R_L} \tag{10}$$

The value of resistance R_L to attain the maximum power is calculated as

$$R_L = 1 / \omega C_p \tag{11}$$

The output power of the monolithic piezoelectric transducer is given as

$$P_{R(\max)} = I_o^2 / 4\omega C_p \tag{11}$$

The PE transducer sandwiched between electrode layers is split into n-regions and the model is analyzed. The current source and inherent capacitance for each individual region can be expressed as I_P / n and C_P/n, because the total area is split into $1/n$ regions. As the regions are connected in series electrically, the equivalent current and capacitance can be expressed as I_P/n and C_P/n^2 respectively and the amplitude of open circuit voltage V_{OC} can be given as

$$V_{OC-n} = \frac{1}{2} \frac{Q_{total} / n}{C_p / n^2} = nV_{OC} \tag{12}$$

The V_{OC} can be increased by the factor n as compared to the voltage produced in the monolithic model and the current is decreased by n times. The current amplitude, when a variable resistor R_L with matching impedance is connected to this model, which can be expressed as

$$I_{R-n(j\omega)} = \frac{I_o}{n} \frac{Z_c}{Z_C + R_L}$$
$$= \frac{I_o n}{n^2 + j\omega R_L C_p} \tag{13}$$

The output power consumed can be calculated as

$$P_{R-n} = \frac{1}{2} | I_R^2 R_L |$$
$$P_{R-n} = \frac{I_o^2 / 2}{(n^2 / R_L) + (\omega^2 C_p^2 R_L / n^2)} \tag{14}$$

The maximum output power for n-region is calculated as

$$P_{R-n(\max)} = I_o^2 / 4\omega C_p \qquad (15)$$

The results show that when the piezoelectric transducer is split into n regions the value of output power remains the same but the value of output voltage is increased n times as compare to the output voltage of the monolithic electrode layer model.

Piezoelectric material produces an AC voltage signal at the output. So, the rectifying circuit is needed to convert the AC voltage signal into a DC voltage signal. For this purpose, rectification is required, where alternating current (AC) is converted into direct current (DC), allowing the flow of electrons in one direction only. There are two major types of rectifiers which are Half Wave Rectification (HWR) and Full Wave Rectification (FWR). In HWR of single-phase supply, only half cycle of AC wave is passed while the other half cycle is left unused. The positive part of the cycle is passed blocking the negative part of the cycle. As only half of the wave cycle is passed reaching output resulting in lower mean output voltage [10]. In FWR of single-phase supply, both positive and negative cycles are rectified. This yields in higher output voltage.

2.4. Conventional Full Bridge Rectifier (Con-FBR) circuit

The Con-FBR circuit is the combination of four diodes. Four diodes are connected in a series labeled as D_1-D_4 as shown in Fig. 8. The diodes D_1 and D_3 work for the positive cycle whereas, D_2-D_4 works for the negative cycle of the AC voltage signal V_{PN} produced by PE harvesters [10-20]. The capacitor is attached parallel to the diodes as C_{RECT} along with load resistance R_{RECT}.
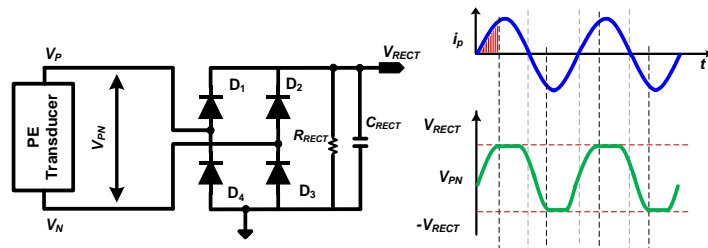

Fig. 8. Schematics of the conventional full-bridge rectifier Con-FBR.

In every half cycle of the input current can be split into two regions in which one part is $t=t_o$ to $t=0$ and the other part is from $t=0$ to $t=t_\pi$. During the first half cycle, the current i_p flows to the input capacitor C_p and charges or discharges it until the voltage V_{PN} becomes equal to $V_{RECT}+2V_D$. The diodes start working, allowing current to flow through the output capacitor C_{RECT}. It keeps on working until the current changes its direction and the second half i-e., the negative part of the cycle begins. In the negative half, the current flows through the output capacitor C_p when V_{PN} reaches $-(V_{RECT}+2V_D)$. The total amount of power that can be extracted from the PE harvester is given by [10-11].

$$P_{RECT,FB}(\max) = 4C_p (V_P - 2V_D)^2 f_p \qquad (16)$$

2.5. Voltage Doubler Rectifier (VDR) Circuit

The voltage doubler is a type of rectifying circuit which has the ability of amplifying the voltage at the output by the factor of two [14]. It consists of just two diodes shown in Fig. 9 where the charge flow to the output capacitor does not occur every half cycle of the input current because of two diodes. The piezoelectric harvester circuit is connected in parallel with the voltage doubler and capacitor C_{RECT} is used to store charges on the output.
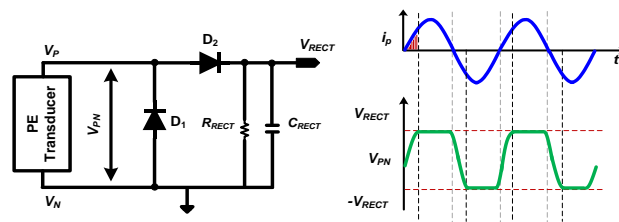
Fig. 9. Schematics of voltage doubler rectifier (VDR).

During the positive half cycle, the input current i_p flows through the input capacitor C_p until it reaches $V_{RECT}+V_D$. Where V_D is the voltage drop of the diode. The diode is then turned on and the current flows through the output capacitor C_{RECT}. During the negative half-cycle, the input current flows through the diode in parallel with the piezoelectric harvester. As a result, the input capacitor C_p is discharged to the ground [12-20]. The total amount of power delivered to the output by the voltage doubler rectifier will be

$$P_{RECT,VD}(\max) = C_p(V_P - V_D)^2 f_p \qquad (17)$$

2.6. Active diode rectifier

In this type of rectifying circuit high speed comparator is used to drive MOSFET as an active diode [12, 13]. It is done by replacing a diode with an actively controlled switching element. It is also known as a synchronous rectifier. The control circuity for active rectification usually have comparators to choose the most suitable voltage among the coming voltages. It can sense the voltage of input AC and open transistors at the correct time to allow current to flow in the correct directions. It allows current to flow in one direction while blocking current to flow in another direction. In this way, it works as an ideal diode. In this technique of active rectifier, the conducting resistance and the voltage drop are much minimized than the Con-FBR circuit. Comparators design with standard CMOS technology provides minimum drop-out voltage along with the small size [14-17].

2.7. Proposed design

The proposed design is shown in Fig. 10. It consists of four diodes. The Diode 1 & 2 work as the p-type while the Diode 3 & 4 work as the n-type in the whole rectifier configuration. It consists of n and p-type MOSFETs and these are operated in the linear region (deep triode region) exhibiting a very small amount of resistance. It has the ability to conduct with minimizing voltage drop for the same value of current. MOSFET is connected in such a way that it conducts only in one direction (forward direction) while blocking the reverse direction (backward direction) thus preventing the reverse leakage of current. This circuit is composed of four diodes. Each diode consists of one NMOS and one PMOS while placing a diode in between p-type and n-type MOSFETs. Diode 1 & Diode 3 will be ON for the positive cycle and Diode 2 & Diode 4 will be ON for the negative cycle. Let us consider the case of 1st half cycle where Diode 1 & 3 are ON.

The voltage extracted from the PE harvester starts to flow such that ($V_P > V_N$) the positive cycle of voltage reaches the diode D_1 which is in the forward direction so it will allow voltage to flow from it and charges the small capacitor C_1 and this voltage can be used to ON the N_1 transistor, which directly connects the gate of P_1 to the V_N which results in the main transistor P_1 ON in first half cycle. The capacitor C_1 maintains the voltage constant to turn ON the N_1 completely. Similarly, for the Diode 3 will be turned ON. In a negative cycle when ($V_P < V_N$), the Diode 2 and Diode 4 will be turned ON in the same symmetric way with the help of the control circuit, which consists of a diode and a transistor. The voltage drop of the main transistor is reduced while blocking the reverse leakage current.
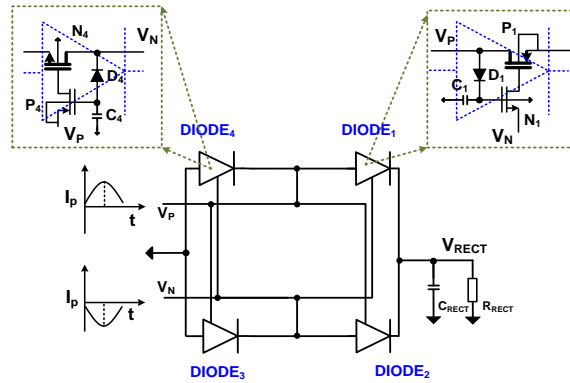
Fig. 10. Schematics of the proposed design.

MOSFETs are made to work in the deep triode region providing $V_{GS}>V_{TH}$. In the small portion of the triode region, there is a linear region in which because of the small value of applied drain-source potential MOSFET works as voltage-dependent resistor, where ohm's law is obeyed i-e., $V = IR$ (voltage is directly proportional to the applied current). This ohmic relationship continues until the voltage reaches a maximum value called as pinch-off voltage. After the triode mode saturation region is started also known as the active mode region, where $V_{DS}>V_{GS}-V_{TH}$.

3. Results and discussion

For comparison, conventional full bridge rectifier (Con-FBR) circuit is simulated as well using an ideal input signal and then it is sourced by the piezoelectric harvester electric model circuit and then the proposed designed is simulated using the same kind of sources. It is observed that the proposed design is more efficient when compared with the Con-FBR. At the same input and load conditions, the output of Con-FBR and Proposed design is 3.5V and 4.8V respectively which definitely results in higher efficiencies.

3.1. Conventional Full Bridge Rectifier (Con-FBR) Results

Fig. 11 shows the results of the Con-FBR using the ideal source and PE electrical model. In Fig. 11(a). It can be seen that the voltage drop at higher load is less while at lower load and the maximum output voltage is obtained, which means that at 5KΩ the circuit is more efficient and at 100Ω load, the circuit has a larger amount of voltage drop resulting in minimum conversion efficiency. The results are better at higher loads using PE electrical model as well as shown in Fig. 11(b).
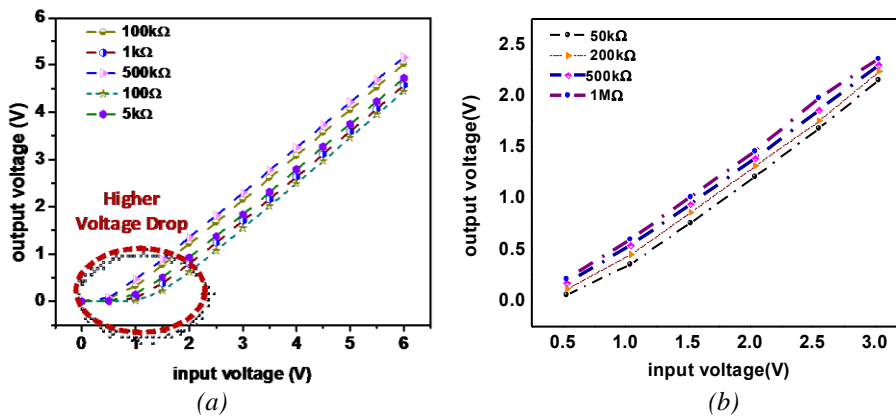

Fig. 11. Input versus output voltage of Con-FBR at different loads Using ideal source (a) Using Ideal Source (b) Using PE electrical model.

Fig. 12 shows the results for the highest peak for the Con-FBR using the piezoelectric harvester. The value of load resistance is 1MΩ using frequency 200Hz. The input voltage is 3V and it gives out the output rectified voltage of 2.8V.
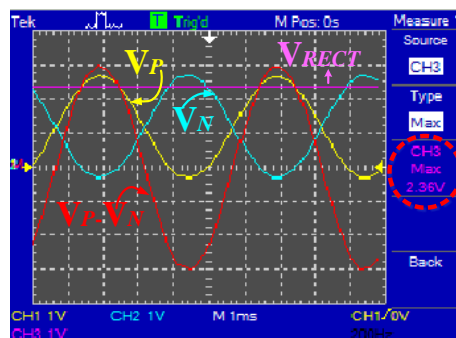

*Fig. 12. Graphical view for output versus input voltage for conventional bridge
rectifier circuit (Con-FBR).*

Fig. 13 shows the graph of input versus output power at different load conditions. It can be seen that the maximum power of 500μW is produced at 50KΩ load resistance. Whereas minimum power i.e. 300μW is produced at the load of 1MΩ. So, the circuit extracts more power at lower loads when connected with a piezo-electric harvester. The power in increasing with the decrease in the load resistance.
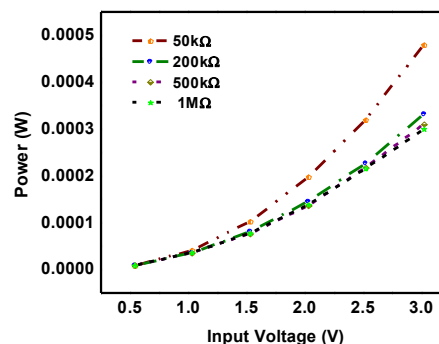

Fig. 13. input voltage versus output power of Con-FBR using the piezoelectric harvester.

3.2. Proposed rectifier design results

The results of the proposed rectifier design are presented here. Figure. 14 shows the graph of input versus output voltage and power at different loads when the ideal source is applied as the input source. In Fig. 14(a), As, the load resistance increases the output voltage also increases. There is a distortion between input voltage range from (0 - 1.25)V, this is because our proposed rectifier design is more efficient at higher nodes and at lower voltages i.e. (0 - 1.25)V, it shows the distortion when the load is between 100Ω to 100KΩ. The maximum power is extracted at 0.5Ω load and is shown in Fig. 14(b). At lower nodes, the value for output power is less but at higher nodes between (2 - 5)V, the value of output power is increasing.
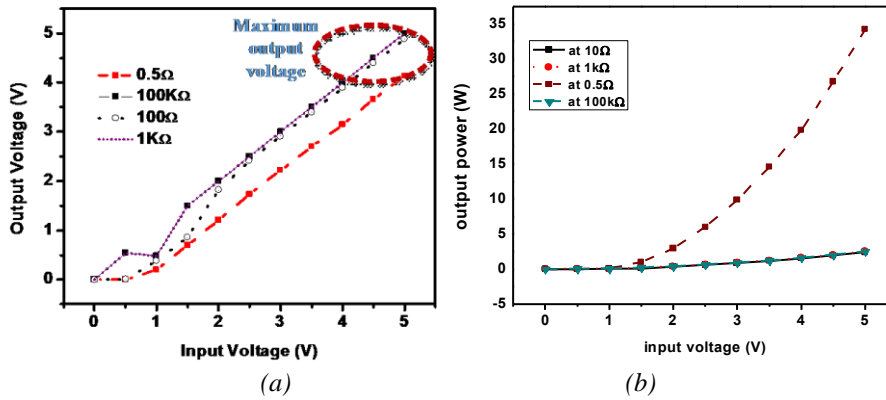
(a) *(b)*

Fig. 14. Proposed rectifier using ideal source at different loads (a) Output voltage versus input voltage (b) Output power versus input voltage.

Fig. 15(a) shows the relationship between input current and output voltage keeping load resistance constant at 250KΩ at different frequencies to find the best frequency figure for operating the proposed rectifier design with the piezoelectric transducer as a source. Figure 15(a) shows that the output voltage increases by increasing the value of input current and decreasing the value of the frequency of the current source. The maximum output voltage is achieved at 100 Hz frequency.
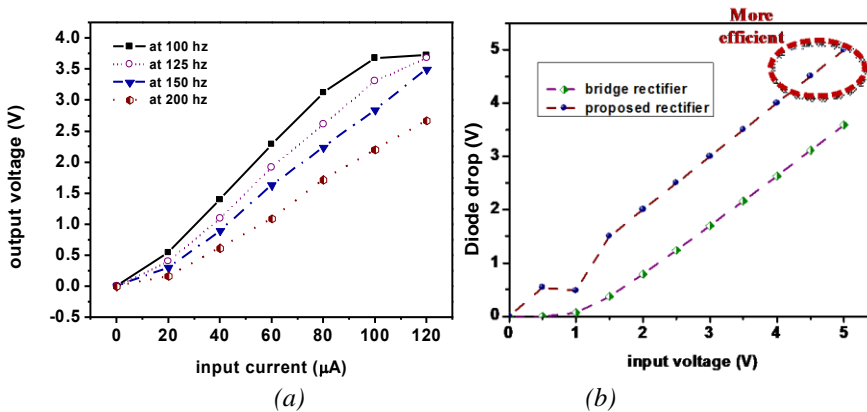

(a) *(b)*

Fig. 15. (a) Input current versus output voltage at different frequencies (b) Input voltage versus output voltage of Con-FBR and proposed rectifier design.

Fig. 15(b) shows that the diode drop of Con-FBR and proposed rectifier is more as compared to our proposed design. It shows that our proposed design is 40 times better than the conventional bridge rectifier at same load conditions. At the input of 5V, the rectified output voltage of the Con-FBR circuit is 3.9V whereas the proposed one is 4.8V keeping the load resistance 1KΩ.

Fig. 16 shows the results for the highest peak for a proposed design using piezoelectric harvester. The value of load resistance is 250kΩ using frequency 100Hz. The input current was 120μA and it gives out the output voltage of 4.4V resulting in the 88% power conversion efficiency while at the same input conditions Con-FBR gives the output voltage of 2.3V.
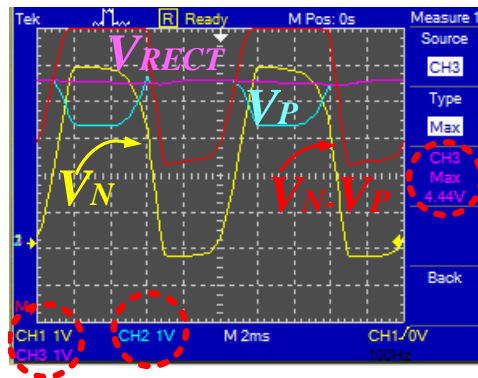
Fig. 16. Graphical view for output versus input voltage for proposed rectifier design.

4. Conclusions

The aim of this research is to minimize the voltage drop in the proposed circuit design with the help of MOSFETs. In conventional full bridge rectifier (Con-FBR) the power losses are very high because diodes have their own voltage drop. To minimize these losses, the Con-FBR circuit is altered with the employment of both N-type and P-type MOSFETs. Each MOSFET is operated in the triode (ohmic) region while blocking the reverse leakage and thus reducing the threshold voltage up to 70%.

Both positive and negative cycles are availed and investigated to extract the maximum output voltage. It is simulated in NI-Multisim (version 14.0) and implemented using discrete components. The circuit simulation results show that the proposed design has a better power conversion efficiency of 88% and can extract power more than four times Con-FBR.

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