STUDY OF NON-IDEAL EFFECTS IN ZnO TFT's

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In this work we report the non-ideal effects on the performance of ZnO-based Thin Film Transistors (TFTs) as an active channel. This TFT was grown by RF magnetron sputtering technique. The transistor structure fabricated in this study consists of ZnO/SiO_2/n-Si/Au-Gate. The TFTs were done under two conditions: depositing the active layer in the substrate with constant temperature of 150°C and with room temperature, both with different channel length of 10, 20, 40 and 80 μm, and constant channel width of 450 μm. In both conditions of temperature for the substrates, a typical behavior of the family curves I_{DS} vs V_{DS} was obtained. Channel length modulation, hot carrier, and long channel are some of the effects that occur in the transistors presented in this research. The motilities, threshold voltage, on/off rates and gate swing voltages were calculated. Also, conductance and transconductance were evaluated for all cases, which are related with non-ideal effects.

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Keywords: ZnO, Transistor, MOSFET,Semiconductor

1. Introduction

Recently, in order to resolve issues related to the low field effect mobility and the opacity of silicon, the research has been focused on the development of transistors with different channel materials. Other semiconductor materials used as active layers are, for instance, Gallium Arsenide, Cadmium Sulphide, Lead Sulphide, among others [1-3]. The main materials under study are transparent semiconductors, such as the materials used in Active Matrix Liquid Crystal Display (AMLCD) or Organic LED ultra-thin screens (OLED displays). These materials are required to avoid the area restrictions and that could be developed all the electronics on the transparent screen [4]. Zinc Oxide (ZnO) Thin Film Transistors (TFT) have attracted the interest of the scientific community due to its special features, such as a wide band gap energy, transparency, and field effect mobility [4-8]. Most of these studies have been done on different substrates, gates, and gate insulators to find an optimal structure ZnO TFTs that meets the minimum requirements for the before mentioned applications [9].

One of the key factors that limits the development and reliability of the devices are thermal issues, therefore it is very important to conduct a systematic characterization of fundamental thermal effects inside single devices, as well as the characterization of non-ideal effects derived from the device structure. For instance, in a SOI MOSFET (Silicon Oxide Insulator

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Metal Oxide Semiconductor Field Effect Transistor), the thick buried-oxide underneath the Si (Silicon) film gives rise to the self-heating effect (SHE), which sometimes results in a negative output conductance.

The purpose of this work is to emphasize the non-linear behavior effects such as transconductance, conductance, short channel, and self-heating presented on a TFT system, built with a RF magnetron Sputtering on SiO_2/Si.

2. Experimental

ZnO films were deposited on an n-type silicon substrate with a thermally grown silicon dioxide film (SiO_2) of 100 nm. An RF magnetron sputtering was utilized to growth the ZnO thin films, using a ZnO target with 99.9% of purity. The system was initialized at $5X10^{-6}$ torr of pressure. The pre-sputtering was done for 5 minutes at 150 watts, in order to clean the target surface. Two different substrate temperatures were considered, 150°C and room temperature. The pressure employed was established by controlling the argon flux at the input and it was kept between at 5-7 mTorr with argon flux range of 45sccm. The deposit power was established at 150 watts for 15 minutes, to deposit ZnO thin film. The drain and source contacts were deposited by e-beam evaporation and patterned by lift off, the common gate was also deposited by e-beam evaporation. The electrical characterization was carried out in dark conditions using a semiconductor parameter analyzer Keithley 4200. The FET scheme developed in this work is shown in figure 1.

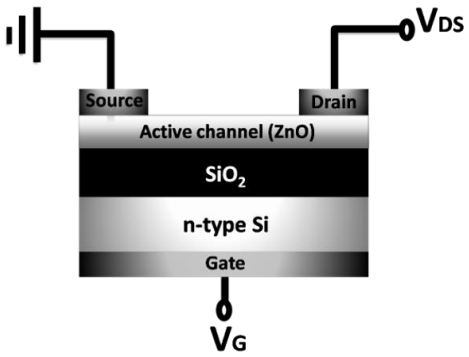

Fig. 1 Schematic cross-section of the bottom-common gate ZnO based TFT configuration

3. Results and discussion

Firstly we present a compilation of characterization realized on the material that we use as the active layer in the two sets of elaborated transistor, in part (a) of Figure 2 is shown the diffraction of X-rays for ZnO films grown with conditions of 150 Watt, 15 minutes at work pressure between 5-7 mTorr with argon flux of 45 sccm; the upper diffractogram corresponds to a substrate without control of his temperature, while the lower diffractogram was obtained when the substrate was maintained at a constant temperature of 150°C. Part (b) of Figure 2 shows the absorption response spectrum in the UV-Vis region of such a ZnO material layer, here is observed that for wavelength in the 440 to 820 nm range, this material has low absorption; from these data was built the inset, based in the Tauc procedure for calculate the optical energy band gap, see part (c) of same figure 2. Finally, the parts (d) and (e) are atomic force micrographs which depict the surface morphology of such a used material.

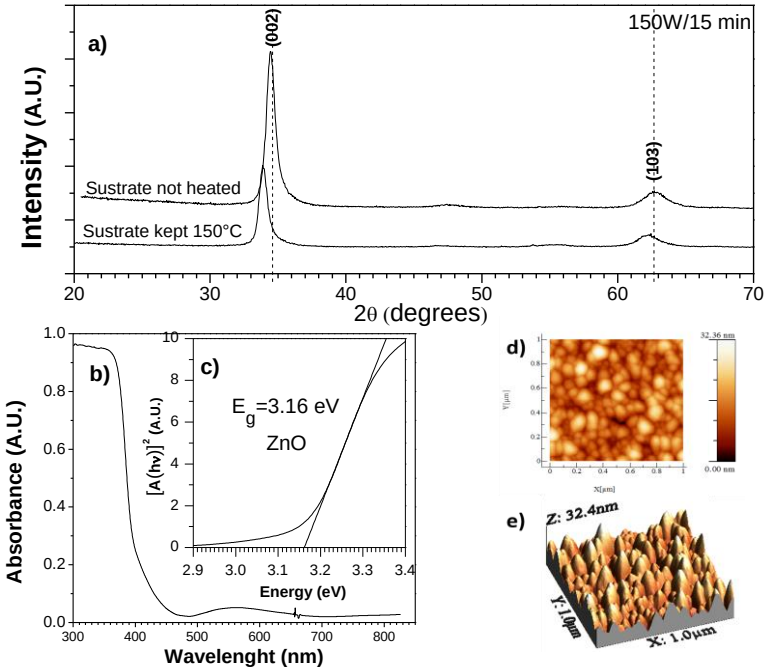

Fig. 2 XRD patterns for two different substrate temperatures a) 150°C and room temperature, b) Absorption response of the ZnO film, c) the inset corresponds to the Tauc Plot for calculate the direct band gap d) and e) AFM images of ZnO thin film deposited during 15 minutes at room temperature

In order to analyze the electrical parameters, one of the most common models correlating several TFT's parameters in saturation region is shown in the Equation (1).

$$I_D = \frac{W\, C_{S_iO_2}\, \mu}{2L}(V_G - V_{TH})^2 \tag{1}$$

Where I_D, V_G and V_{TH} are drain current, gate voltage and threshold voltage; W, L and $C_{S_iO_2}$ are wide and length of the channel, and the silicone dioxide capacitance, respectively. The $C_{S_iO_2}$ is the capacitance per unit area and is calculated by the following expression:

$$C_{S_iO_2} = \frac{\varepsilon_0\, \varepsilon_{S_iO_2}}{t_{S_iO_2}} \tag{2}$$

Here, ε_0 and $\varepsilon_{S_iO_2}$ are the vacuum and the zinc oxide permitivitties, respectively, and $t_{S_iO_2}$ is the oxide thinckness. From equation (1), the equation (3) is obtained:

$$\sqrt{I_D} = \left(\sqrt{\frac{W\, C_{S_iO_2}\, \mu}{2L}}\right) V_G - \left(\sqrt{\frac{W\, C_{S_iO_2}\, \mu}{2L}}\; V_{TH}\right) \tag{3}$$

Which is used to evaluate

$$\left(\sqrt{\frac{W\, C_{S_iO_2}\, \mu}{2L}}\right) \equiv m \tag{4}$$

and

$$-\left(\sqrt{\frac{W\, C_{S_iO_2}\, \mu}{2L}}\; V_{TH}\right) \equiv b \tag{5}$$

by means a data linear fit to the graphs obtained. So, from equations (1) and (4) we can calculate the field effect mobility leading to the next result:

$$\frac{2L}{w\, C_{S_iO_2}}\left[\frac{\sqrt{I_D}}{(V_G - V_{TH})}\right]^2 \equiv \mu = \frac{2L}{w\, C_{S_iO_2}}(m)^2 \tag{6}$$

The last equations describe a TFT ideal behavior. However, in the practice a non-ideal response is common. The drain-source current presents nonlinear second order effects, such as mobility degradation, channel length modulation (CLM) due short channel, and the impact ionization, among others. These effects can be represented as current gradients of the drain-source current. In order to obtain an I_{DS} expression that includes the nonlinear effects of the drain-source current, the derivation needs to be considered in two dimensions. So, the drain-source current should be recalculated considering a correction to the equation (1):

$$I_{DS} = \frac{W\, C_{S_iO_2}\, \mu}{2L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{7}$$

Where $(1+\lambda V_{DS})$ is the correction term. The factor $1/\lambda$ is the intersection of the current graphs extrapolated [10]. Owing to CLM the drain current varies with the drain-source voltage. This current gradients are involved with the conductance (g_D) and transconductance (g_m) definitions, and a first approach using

$$g_m = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_D = Const.} = \frac{1}{R_{DS}} = C_{S_iO_2}\mu\frac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) \tag{8}$$

$$g_D = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_G = Const.} = \frac{W\, C_{S_iO_2}\, \mu}{2L}(V_{GS} - V_{TH})^2\lambda \tag{9}$$

From this mathematical background, the results are analyzed and presented as follows.

The fig. 3 shows a set of results corresponding to semi-logarithmic I_D versus V_G and I_D square root versus V_G, for the group of Pseudo MOSFET's where the ZnO channel was grown at 150°C. The dashed lines correspond to linear fits of the data, which determine the threshold voltages involved with equations (1) and (7), the obtained values were between the 17.5 - 20.6V range. The solid lines correspond to linear fits which mark the subthreshold region, from where the gate-voltage swing (S) are calculated through the inverse slope, these values were, 11, 14, 16 and 20 V/decade for channel lengths 10, 20, 40 and 80 μm respectively. The field-effect mobility had the same value of 0.001 $cm^2V^{-1}s^{-1}$ for all channel lengths. The insets display family plots of drain current curves as a function of the drain–source voltage, keeping the gate voltage constant as it is indicated, for values between 0 - 40 V range whit 10V steps.

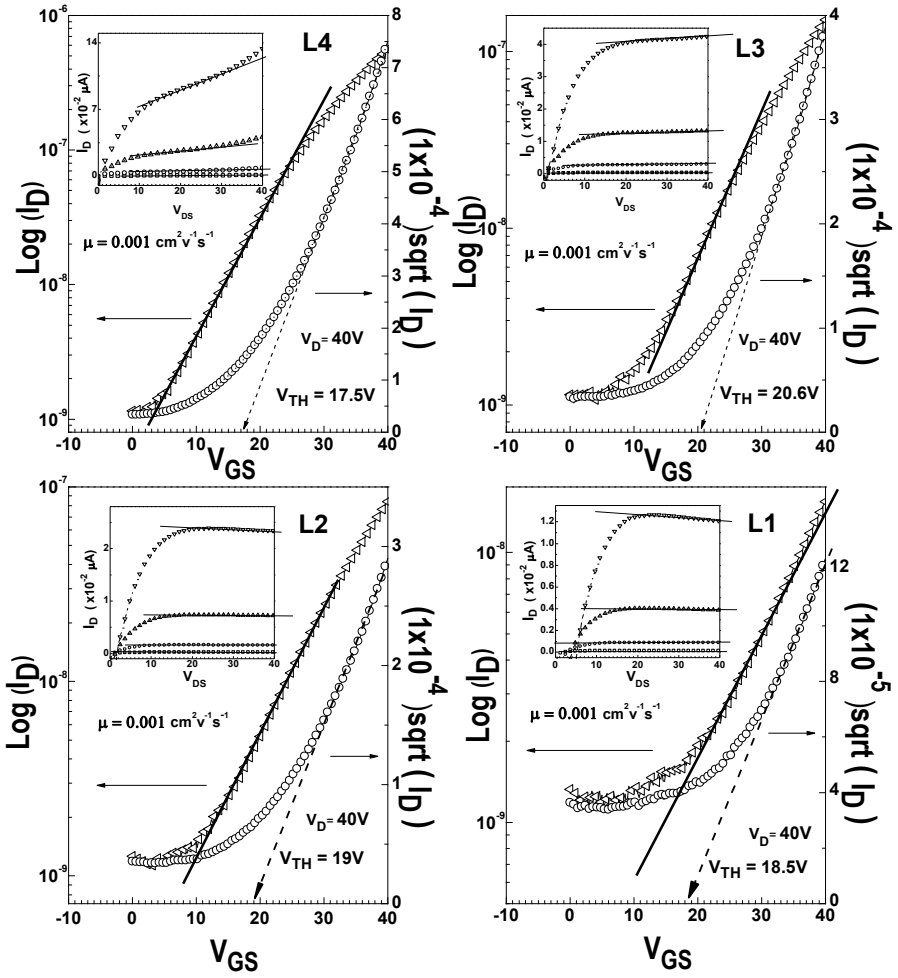

Fig. 3 Plots of log (I_D) vs. V_{GS} (left scale) and $(I_D)^{1/2}$ vs. V_{GS} (right scale), in order to measure the swim and the threshold Voltages. The inset displays family curves of drain current $I_{DS} \equiv I_D$ as a function of drain–source voltage $V_{DS} \equiv V_D$ for some selected values of gate voltages $V_{GS} \equiv V_G$, for the TFT´s where the ZnO channel was grown at 150°C

In the same way, the fig. 4 shows a set of graphs corresponding to semi-logarithmic I_D versus V_G and I_D square root versus V_G, for the group of Pseudo MOSFET´s where the ZnO channel was ground at room temperature. The dashed lines correspond to the linear fits of the data which determine the threshold voltages, the obtained values were between 19-20V range. Furthermore, the solid lines correspond to linear fits which mark the subthreshold region, from where the gate-voltage swing are l9, 11, 13 and 15 V/decade for channel lengths 10, 20, 40 and 80 μm, respectively. The field-effect mobility values were between 0.001 to 0.003 $cm^2V^{-1}s^{-1}$ range from the saturation region. The inset display family plots of drain current as a function of the drain–source voltage, keeping constant the gate voltage as it is indicated, for the values between 0-40 V range.

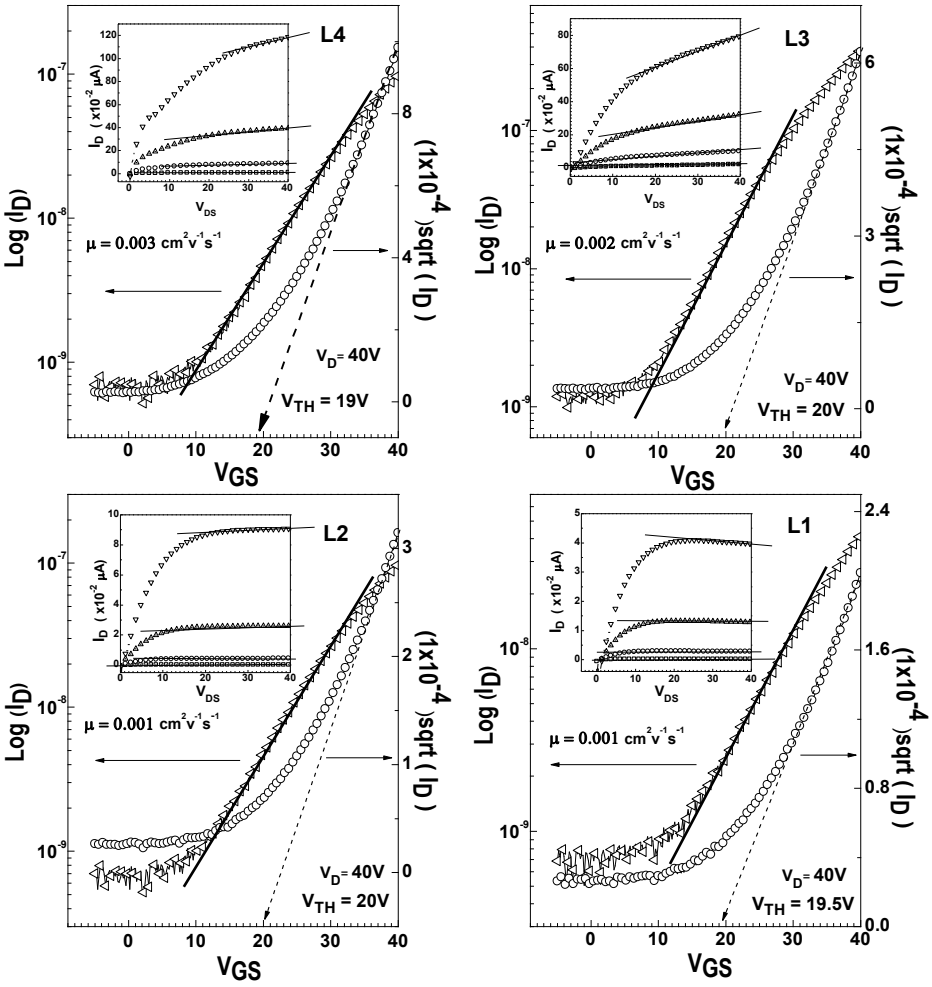

Fig. 4 Plots of log (I_D) vs. V_{GS} (left scale) and $(I_D)^{1/2}$ vs. V_{GS} (right scale), in order to measure the swim and the threshold Voltages. The inset displays family curves of drain current $I_{DS} \equiv I_D$ as a function of drain–source voltage $V_{DS} \equiv V_D$ for some selected values of gate voltages $V_{GS} \equiv V_G$, for the TFT´s where the ZnO channel was grown at room temperature

To correlate some features of the devices with its calculated parameters, we can observe that increasing V_d the channel acts as resistance where the drain current is directly proportional to such V_d. If V_d continues increasing this leads to increases the depletion region close to the drain and consequently the drain current decreases going to a saturation current [11]. In our results three interesting cases were presented, the first one, for short channel lengths L_4 y L_3, drain current increases after a saturation voltage (V_{sat}), i.e., if $V_d > V_{sat}$ the pinch-off point gradually moves toward the source, the reason of this behavior is that the effective channel length diminishes. This phenomenon is called as channel length modulation [11-14]. The second case is presented under CLM, when again the drain conductance increases significantly with the drain voltage due to high energy electrons called hot carrier [12-17].

For channel length L_2 y L_1 a better saturation curves were obtained. The third important case to note was a negative saturation conductance, this is attributed to self-heating induced by dc current employed to obtain the characteristics curves [18-20].

From the insets, the family curves in figures 3 and 4, the transconductance and conductance are calculated and depicted in Figures 5 and 6. Particularly, the conductance was obtained from the slope of solid line in the insets family curves, in the saturation region. On the other hand, the transconductance (g_m) was calculated by means of discrete derivative of the current

in the saturation region for two consecutive curves I_{DS} vs. V_{DS} with a different V_G; this difference is known as step.
The transconductance g_m is considered as the gain and can be obtained using the next equation:

$$g_{m2} = \frac{I_{DS\,2} - I_{DS\,1}}{V_{G\,2} - V_{G\,1}} \tag{10}$$

Where g_{m2} is the gain produced by a V_G step, for the complete set of our transistors see Fig. 4.

Summarizing, in a conventional MOSFET, the drain current remains constant in the saturation region, but in this case, the drain conductance shows an increase with the drain voltage, that means that at some point along the channel, the local potential difference between the gate and the oxide-silicon interface is not enough to support an inversion layer [14]. This effect can be remarked by the self-heating device which may show as conductance ratio increase or conductance ratio decrease as a function of the voltage and the channel length, this may be seen in figure 5. This electrical potential field together with the current flow along the channel generates a non-uniform temperature distribution, which is usually located towards the drain end for a typical MOSFET [21].

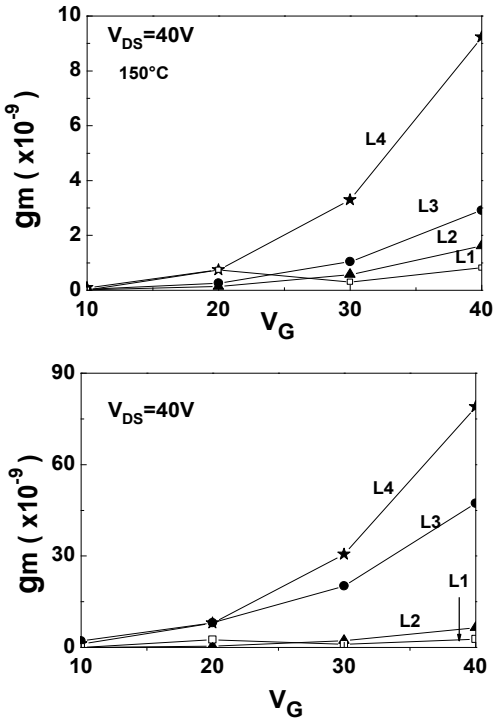

Fig. 5 Transconductance: At the top the channel was grown at 150°C and bottom the channel was grown at room temperature.

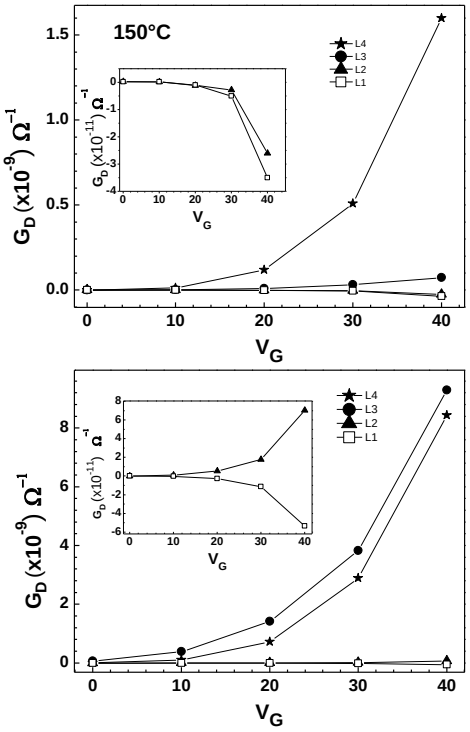

Fig. 6 Conductance: At the top the channel was grown at 150°C and bottom the channel was grown at room temperature

In Fig. 5, in the up it is shown the case where the ZnO channel was grown at 150°C and down the case where the channel was grown at room temperature. In both cases L_4 and L_3 present a growing behavior; the insets correspond to a scales magnification for L_1 and L_2 in order to observe the g_d evolution.

4. Conclusions

This study demonstrated the possibility of changing the behavior of ZnO thin-film transistors by controlling the channel lengths or the thickness using a simple and low-cost process at room temperature or heating the substrate, which is a valuable result for the research related to the fabrication of electronic devices.

Also the electric characterization of ZnO TFT's have been evaluated both in the linear and saturation regions. Furthermore the small-signal parameters, like the transconductance and the drain conductance have been evaluated in the saturation region.

Three anomalous cases of current were observed experimentally in the output characteristics of our TFT's at high V_{DS}. The results of both sets cannot be compared in terms of the current levels because the temperature substrate conditions get different channel thickness. Self-heating in ZnO TFTs can result in an overestimation of field-effect mobility in the saturation regime from heating induced current increases, self-heating can also lead to a thermal runaway device failure mechanism.

Finally, it is important to note that the structure of the devices affect the results, the amount of charge is distributed in the common gate, but only a little ratio of majority carrier can be transported in each transistor. It is known that the on/off current ratio is better when the structure characteristics are well determined like an independent gate for each device, located justly between the source and drain.

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