Performance analysis of OTFT with varying semiconductor film thickness for future flexible electronics

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The goal of this study was to get a deeper understanding of the intricate impact of organic semiconductor thickness on the performance of devices, using a thorough and meticulous investigation at the microscopic level incorporating the density of defect model using using Silvaco ATLAS TCAD Simulator. The present work thoroughly investigates the relationship between the thickness of semiconductors and important performance parameters, such as hole concentration, electric potential, electric field, and Hole QFL. The comprehensive insights derived from this research not only enhance the comprehension of device physics but also provide a framework for the systematic enhancement of electronic devices. The widespread use of organic thin film transistors (OTFT) in future Flexible electronics, particularly in display and memory circuits, necessitates the incorporation of low voltage, high speed, and low cost characteristics.

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1. Introduction

Over the last couple of decades, OTFTs have been used for a broad variety of purposes, including inexpensive displays, organic memory, important radio frequency tags, polymer circuits, and sensors [1-4]. For practical, commercial uses, threshold voltage, mobility, transconductance, and current in the device provide the biggest challenge for organic devices [5]. The particle size of the OSC thin film, the trap state, and the thickness of the semiconductor layers may all influence these parameters [6,7]. In this study, we investigate the influence of varying the active layer thickness on a variety of physical parameters, including the distribution of charge carriers, the electric field, the concentration of holes, and the holes' quasi-Fermi level (QFL). Electrical parameters such as the on-off current ratio, mobility, and threshold voltage are all influenced by the active layer thickness. The on-off current ratio, mobility, and threshold voltage are all electrical properties of OTFTs that are affected by the thickness of the active layer, in addition to the physics-based factors. Although the bulk current is what primarily affects the on-current, the off-current also increased with the rise in semiconductor thickness. The off current should be relatively minimal as it has a direct relationship to power consumption and also affects the switching behavior of the device. Off-current reduction is especially important in memory and displays devices with thinner active films. Altering the thickness of the active layer used to create OTFTs is one method for enhancing their functionality. Due to charge localization, understanding the study of the semiconductor layer and the semiconductor-dielectric interface is crucial for enhancing device performance [8-13]. Defects at the interface level drastically reduce the device's performance. In this way, the thickness of the semiconductor layer is a critical factor in the functionality of the device. A portable device's power needs may be better met with a lower threshold voltage (V_{th}). From a deep device physics perspective, this research explores the effects of changing the thickness of the semiconductor layer on several electrical parameters. There is strong evidence that organic semiconductors may serve as a direct replacement for amorphous silicon (a-Si) in active matrix displays based on thin-film transistors (TFTs). Electronic circuits

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and devices may now be constructed using the emerging field of flexible electronics, which allows for the integration of electronics onto previously inflexible substrates including paper, plastic, and fiber. When it comes to mass production at a reasonable price, organic electronic materials much outshine their inorganic counterparts. Large-area electronic devices such as organic thin-film transistors (OTFT), organic light-emitting diodes (OLEDs), organic solar cells (OSCs), etc., have been produced thanks to research into organic semiconductors. Since the internal transit of charge carriers essentially controls the performance of an OTFT, the semiconductor layer is crucial to the technology. The active layer and interface at the dielectric have been the focus of the majority of research efforts. There is still a lack of precise comprehension from a deep physics perspective because of the limits of experimental evidence. Several layers of complexity are involved in transistor functioning. Analysis based only on experimental data makes it difficult to understand the underlying physics of the gadget. Learning about the device's microscopic behavior was greatly aided by two-dimensional physical numerical modeling. Two-dimensional simulation makes it simple to investigate a wide range of physical variables that might otherwise be challenging to grasp from experimental data alone. Two-dimensional numerical simulation is used for the in-depth study of physical quantities and electrical parameters. Understanding the device's fundamental operations and figuring out how to optimize its structure may benefit from a two-dimensional simulation of the device.

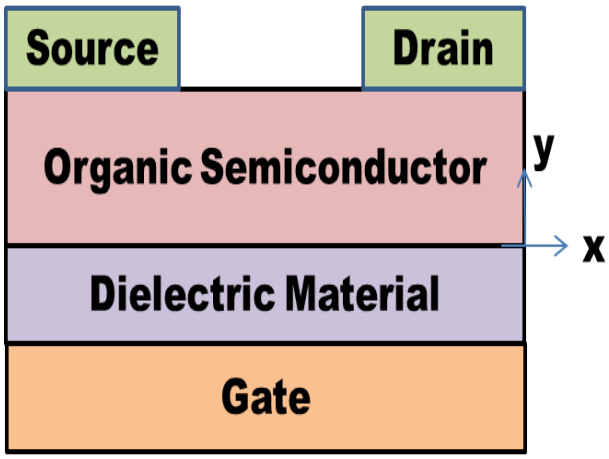

Fig. 1. BGTC structure of OTFT showing x,y distance along the thickness of semiconductor layer.

2. Simulation theory and modelling

Device simulator ATLAS (SILVACO) uses the finite element technique to do a numerical simulation in two dimensions. The continuity equation, Poisson's equation, and the drift-diffusion equation for electrons and holes are all solved by the simulator. We have modeled BGTC pentacene-based OTFTs with varying organic semiconducting material thicknesses (t_{osc}), as shown in Fig. 1. Pentacene is an organic semiconductor with thicknesses ranging from 90 nm to 18 nm. For the transistors and circuits to function at a low voltage of roughly 3V, it is anticipated that the gate dielectric (4.3nm) is extremely thin, resulting in a significant capacitance per unit area. The OTFT features a 20 µm long channel and a 200 µm wide channel. The modeled structural properties of devices are listed in Table 1 . Pentacene semiconductor material features are summarized in Table 2. Poisson's equation and other fundamental device equations may be solved concurrently to determine the physics of a specific ATLAS simulation [14-17]. The creation and propagation of polarons are crucial to the organic semiconductor's physical characteristics [18]. Based on the motion of the carriers within the device and the concentration of the fixed charges, the electric field strength is calculated using the Poisson equation [19][20].

$$\nabla . E = \frac{\rho}{€} \tag{1}$$

where ∈ the permittivity of the region and ρ is the charge density.

For studying the physics of trap states of organic semiconductor layers Gaussian density of defect states model is used in simulations. An electron trap is a defect in an organic semiconductor that creates localized states that are energetically and spatially distributed around the defect site in the semiconductor bandgap. According to their relative energy position from the edge of the band, traps can be classified into two types: shallow traps and deep traps. Traps can be deep if they are located farther from the edge of the band or shallow if they are located near the edge of the band [6]. Using the total distribution density of defect states D(E) containing a total of four bands (two deep (Gaussian) bands and tail (shallow) energy level bands) can be modeled [13][21-22] as it is given as per the following equations (2)–(5).

$$D(E) = D_{GA} + D_{GD} + D_{TA} + D_{TD} \tag{2}$$

where

$$D_{TA}(E) = N_{TA} \exp\left[\frac{E - E_c}{W_{GA}}\right] \tag{3}$$

$$D_{TD}(E) = N_{TD} \exp\left[\frac{E - E_v}{W_{TD}}\right] \tag{4}$$

$$D_{GA}(E) = N_{GA} \exp\left[-\left[\frac{E_{GA} - E}{W_{GA}}\right]^2\right] \tag{5}$$

$$D_{GD}(E) = N_{GD} \exp\left[-\left[\frac{E - E_{GD}}{W_{GD}}\right]^2\right] \tag{6}$$

Trap energy (E), valance energy band (E_V), and conduction band energy (E_C), in which subscripts (D, A, T, G) represent the donor, acceptor, tail & Gaussian states respectively. $N_{TA,}$ $N_{TD,}$ W_{TD} & W_{TA} are acceptor tail states density, donor tail states density, characteristic decay energy of donor tail states & characteristic decay energy of acceptor tail states. $N_{GA,}$ $N_{GD,}$ W_{GD} & W_{GA} are acceptor Gaussian density, donor state Gaussian density, acceptor decay energy & donor decay energy for Gaussian distribution. E_{GD} and E_{GA} are peak energy for Gaussian distribution for donor and acceptor respectively.

This ATLAS simulation uses the Poole-Frenkel mobility model to describe the hopping-based charge transport mechanism in organic materials like pentacene. In the Pool-Frenkel model, charge carriers conduct owing to the greater excitation of trapped carriers by the electric field. The Poole-Frenkel mobility model [24] is used, which may be stated mathematically as follows:

$$\mu(E) = \mu_0 \exp[-\frac{\Delta E_a}{kT} + (\frac{\beta}{kT} - \gamma)\sqrt{E} \tag{7}$$

where, The field-dependent mobility is denoted by (E), the zero field mobility by μ_0, the zero field activation energy by ΔE_a, the Poole-Frankel factor by β, and the fitting parameter by γ. E stands for the electric field, K for the Boltzmann constant, and T for the temperature.

Table 1. Device dimensions for numerical simulation.

Parameter	Value
Semiconductor thickness of pentacene (t_{osc})	Varying from 90 nm to 18nm
Length of Channel (L)	20 µm
Width of Channel (W)	200 µm
Source & Drain Contact Thickness	20 nm
Dielectric Thickness (SiO_2)	4.3 nm

Thickness Of Aluminum	20nm

Table 2. Simulation parameters of the OTFT.

Material parameters	Value
DOS for conduction band(N_C)	2.8×10^{21} cm^{-3}
DOS for valance band (N_V)	1.0×10^{21} cm^{-3}
Permittivity of pentacene	4
Band Gap of pentacene at 300K	1.8 eV
Zero field mobility of the hole	0.85 cm^2/V-s
Pool frankel factor of hole (β_h)	7.758×10^{-5}eV$(V/cm)^{1/2}$
ΔE_a is the zero-field activation energy	1.792×10^{-2} eV

3. Results and discussion

The physical & electrical characteristics of the device of different active layer thicknesses are studied in this section. The two-dimensional finite element method is used for device simulation. To accurately analyze OTFT for different active layer thicknesses, the device simulation includes a hopping mobility model of mobility degradation.

Fig. 2. shows an output characteristic of a bottom-gate top contact OTFT based on pentacene, using SiO_2 material as the dielectric at the gate voltage, V_{GS} = -3.0V, for variable pentacene thickness 90, 65, 32, and 18nm respectively. The simulation parameter is used as given in Table 2. The simulated result of the drain characteristic shows that with an increase in pentacene thickness the drain current increase monotonically. As shown in Fig. 3. , it is observed that the drain characteristic of the simulated device is significantly affected by varying active layer thickness of pentacene. A high on-off ratio of current is also required in display and memory-based circuits. On-current 4×10^{-5} A for 18nm is optimized which is enough to drive various OTFT-based electronic devices.

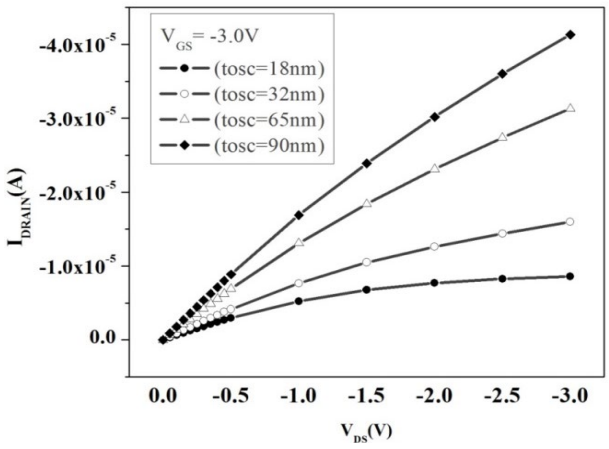

Fig. 2. Drain characteristics for the simulated device with varying thickness of pentacene (90nm-18nm) at V_{GS} =-3.0V.

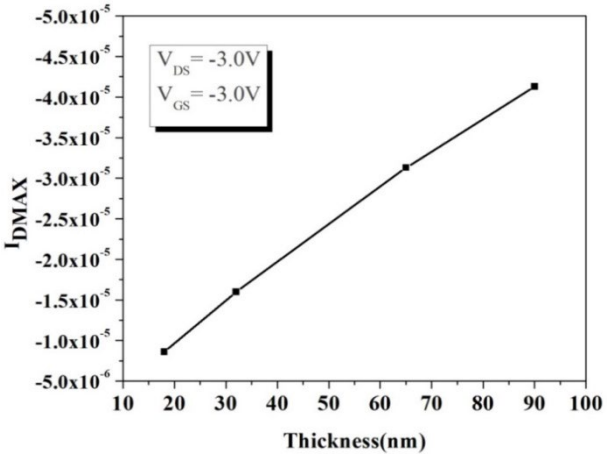

Fig. 3. Extracted drain current varying with pentacene thickness of 90nm to 18nm at V_{DS} = -3.0 V

A potential difference exists between the monolayers of OSC and pentacene because of the electric field that has been generated in the OSC. Charge localization increases close to the surface of the dielectric field as a result of the greater electric field created by the thinner active layer. Fig. 4 shows that the magnitude of the electric field varies with the semiconductor thickness from 18 nm to 90 nm, with values of 1.18×10^5 (V/cm), 9.0 104 (V/cm), 7×10^4 (V/cm), 5.4×10^4 (V/cm) at 18 nm, 32 nm, 65 nm, and 90 nm, respectively.

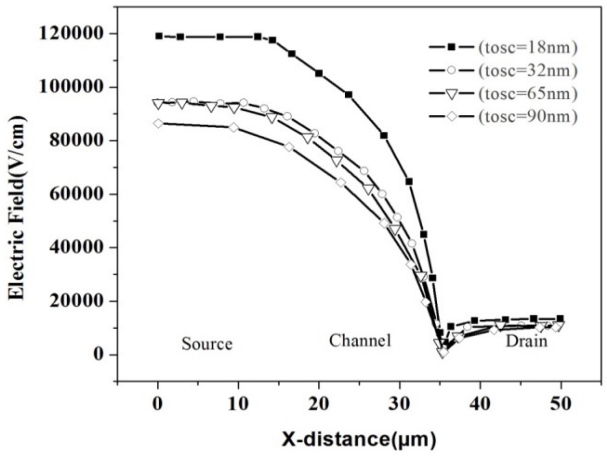

Fig. 4. Electric field at 1 nm below along the x-axis in the semiconductor-dielectric interface.

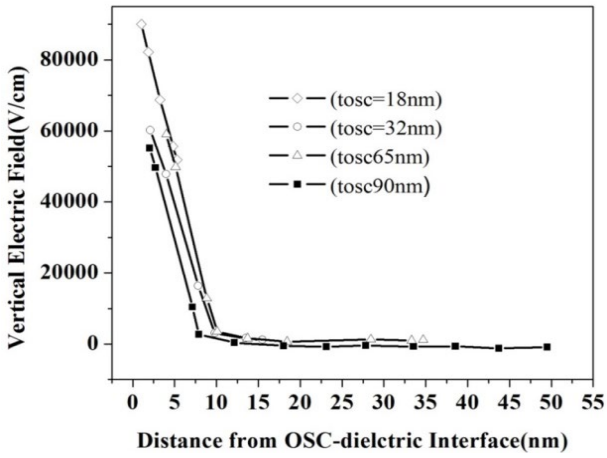

Fig. 5. Vertical Electric field profile along y-distance in structure.

Since relatively few charge carriers at the dielectric interface travel through the impact of self-trapping, as seen in Fig. 5., the vertical electrical field decreases as t_{osc} increases from (18nm to 90nm), leading to an increase in mobility. The magnitude of the vertical electric field is essentially the same at 32 nm, 65 nm, and 90 nm, but moves away from the semiconductor dielectric interface at each of these distances. It describes how charge builds up slightly away from the dielectric's surface such that carriers of the built-up charge encounter less trapping owing to dipoles in that area. When compared to devices with a thinner active layer, this is indicative of a performance boost.

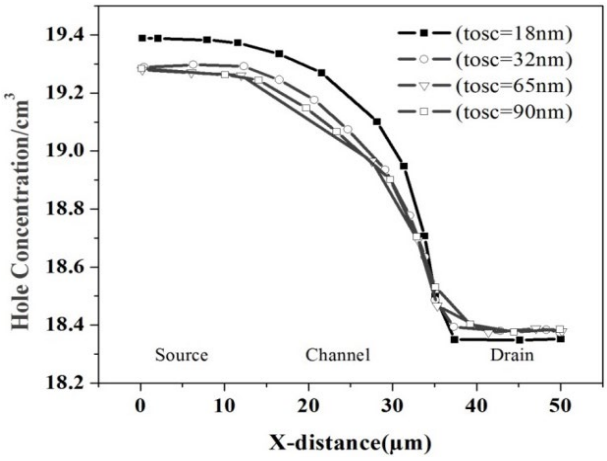

Fig. 6. Hole concentration (h+) along x-distance at 1 nm above the OSC-dielectric interface

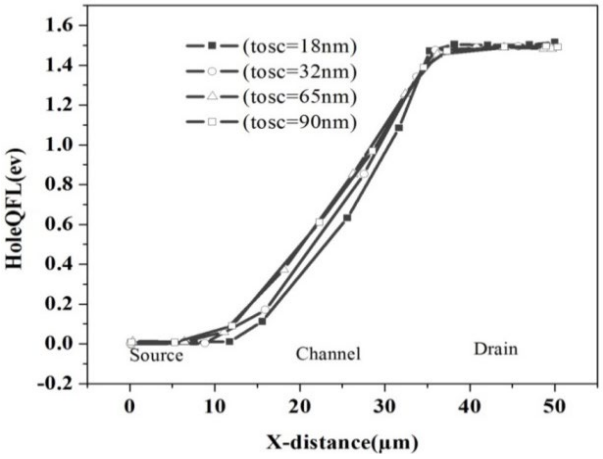

Fig. 7. Hole Quasi Fermi level along x-distance at 1 nm above the OSC-dielectric interface.

Since relatively few charge carriers at the dielectric interface travel through the impact of self-trapping, as seen in Fig. 5., the vertical electrical field decreases as t_{osc} increases from (18nm to 90nm), leading to an increase in mobility. The magnitude of the vertical electric field is essentially the same at 32 nm, 65 nm, and 90 nm, but moves away from the semiconductor dielectric interface at each of these distances. It describes how charge builds up slightly away from the dielectric's surface such that carriers of the built-up charge encounter less trapping owing to dipoles in that area. When compared to devices with a thinner active layer, this is indicative of a performance boost. Because the average charge decreases with increasing active layer thickness, this occurs. Because the electric field intensity between the source (S) and Drain (D) electrodes affects the mobility dependency on current. OSC mobility is field-dependent since it is known to increase with gate voltage (V_{GS}) as shown by the equation (4).

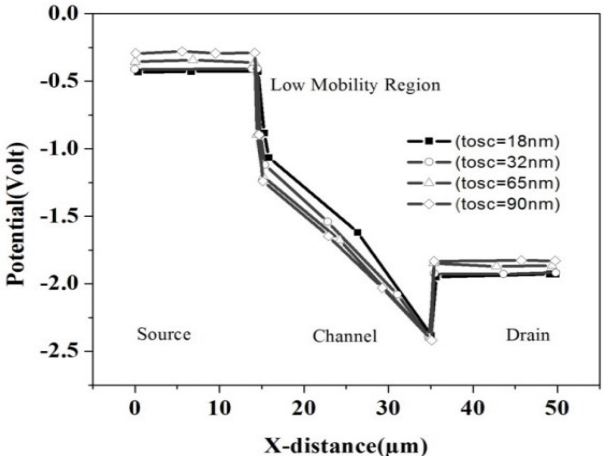

Fig. 8. Surface potential profile 2 nm above the active layer (source, drain, and channel lie between 0–15 nm, 15–35 nm, and 35–50 nm, respectively).

A large buildup of charge carriers at the OSC-dielectric interface causes the mobility to rise as the voltage overload (V_{GS}-V_{th}) grows. Fig. 6. shows that when the applied voltage (V_{GS}-V_{th}) is raised, the hole concentration rises, and as the thickness of the active layer decreases, the electric field rises even at a fixed voltage (V_{GS}-V_{th}). After then, as illustrated in Fig. 7. the hole splits at the Quasi-Fermi level at the dielectric interface.

Initially injected into the device at the source contact, current travels through the semiconductor layer, over the dielectric interface, and exits the device at the drain terminal. Some voltage loss occurs in the contact area and the channel region generated by the concentration of charge carriers above 1 nm from the insulator interface due to the current injection/extraction process. The source, channel, and drain voltage drop profiles are shown in Fig. 8. The foregoing findings indicate that the potential also affects the behavior of the device across a wide range of active material thicknesses.

4. Conclusions

In this work, we simulate low-voltage pentacene-based OTFT devices using the finite element method (FEM). With the aid of a field-dependent mobility model and the density of defects states, we examine how the thickness of the semiconductor affects many deep physics-related parameters and electrical parameters of the device. Basic electrical parameters like threshold voltage, mobility, and maximum drain currents are studied alongside more in-depth physics concerns like the effect of active layer thickness on current flow lines, hole concentration, electric field, vertical electrical field, hole QFL, and potential profile. For many uses, including inexpensive displays and RFID tags, it is crucial to be able to precisely regulate the thickness of the active layer, which is responsible for the relevant physics and electrical parameters.

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