

## PERFORMANCE EVALUATION OF SCREEN-PRINTED C-Si SOLAR CELLS FABRICATED BY THE SIMPLE AND LOW-COST PROCESS

S. M. AHMAD<sup>a,b\*</sup>, C. S. LEONG<sup>a</sup>, K. SOPIAN<sup>a</sup>, S. H. ZAIDI<sup>a</sup>

<sup>a</sup>*Solar Energy Research Institute, Universiti Kebangsaan Malaysia, Bangi, Selangor, 43600, Malaysia*

<sup>b</sup>*Department of physics, Faculty of Science, University of Mosul, 41002 Mosul, Iraq*

Increase the efficiency and reduce the fabrication cost of silicon solar cells represents a challenge to increase the spread of solar cells on the market, the global economic crisis the focus on reducing the fabrication cost with getting good efficiency have increased. In the present work, Sodium hydroxide (NaOH) or Potassium hydroxide (KOH) were employed to cleaning and remove saw damage from as-cut wafers as potential replacements for time-consuming and expensive standard RCA clean. Also, KOH/IPA texturing process was used to create random pyramid features to reduce reflection as well as enhance light absorption. Furthermore, Back to back (B2B) phosphorous diffusion process was used in the fabrication to form n-type emitter layer at four different diffusion temperatures and designed as the in-situ oxide layer passivation process. In order to avoid wet-chemical step, eliminate the need for anti-reflection coating, and enhance manufacturing process throughput. Also, the effect of different emitter sheet resistance ( $R_{sh}$ ) and peak firing temperature of three firing systems on the performance of the cells was investigated. The conversion efficiency, open-circuit voltage ( $V_{oc}$ ), short-circuit current density ( $J_{sc}$ ) and fill factor of  $10\text{ cm}^2$  mono-crystalline silicon solar cell fabricated using the above-mentioned processes were a maximum of ~13%, 590mV, 29.7mA/cm<sup>2</sup> and 73%, respectively.

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### 1. Introduction

Crystalline silicon solar cells are presently the predominant method of photovoltaic power generation. This is due to the combination of comparatively high conversion efficiency, long term stability and optimized manufacturing techniques [1,2]. The major limitations are related to cost and performance [2]. Therefore, the development of fast and cost-effective crystalline silicon solar cells processing technologies plays a key role in the large-scale penetration of photovoltaic in the total energy system [3].

Emitter diffusion is one of the most critical processes in determining the performance of screen printed solar cells for industrial production. On the one hand, a very heavily diffused emitter with a deep junction will create a dead layer near the surface that results in a poor spectral response in cells for short wavelengths of light. At the other extreme, if the emitter is diffused too lightly or if the junction is too shallow, problems result in a poor ohmic contact between the Ag paste and the emitter layer [4]. However, in the crystalline silicon solar cells, make ohmic contact between metal paste and emitter is necessarily to enable carriers into and out of diffused layer without power loss. One of the methods to form ohmic contact, increasing the emitter surface doping to enable tunnelling of electrons from conduction band [5] in addition to other methods as in references [6,7]. For silicon solar cells the typical emitter doping concentration of  $1 \times 10^{18}\text{ cm}^{-3}$  to  $1 \times 10^{20}\text{ cm}^{-3}$ [8]. POCl<sub>3</sub> diffusion is commonly used for emitter diffusion [9]. the emitter made by

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\*Corresponding author: samirasia60@yahoo.com

the  $\text{POCl}_3$  diffusion process are governed by the diffusion parameters like temperature, process duration, and flow rate of  $\text{POCl}_3$ , etc. but it has a strong dependence on temperature because of diffusivity which itself has an exponential dependence on temperature [10].

Firing process is one of the important factors for determining characteristics of the solar cell. In a case of front metallization using screen printing method, the over-fired front contact has an effect that creates a shunting path which is critical for the fill factor of a solar cell by crystallite through emitter. On the other hand, less-fired front contact occurs in high contact resistance due to insufficient contact formation. Moreover, this firing process is also important to back side metallization using screen printing. After firing process on back side metallization, back surface field (BSF) is formed between the crystalline silicon wafer and Al back contact [11]. An Al back contact must fulfil many requirements, including (a) Forming a deep uniform  $\text{P}^+$  region (typically  $> 10 \mu\text{m}$ ) to serve as an effective BSF for minority-carrier reflection; (b) Creating a low-resistance ohmic contact to achieve a high fill factor in the cell; (c) Producing a smooth, bump-free surface to facilitate reliable packaging; and (d) Producing an optically reflective Si-Al interfaces for effective light-trapping. These requirements demand a strong (i.e., higher temperature and longer time) firing cycle [11]. This is usually done in using multi zone-based conveyor belt furnace [2,6,12-15] or single wafer RTP furnace [16, 17]. These industrial-grade furnaces are expensive and consume excessive electricity. We have been developed a two simple rapid thermal annealing (RTA) systems: custom-designed three zone quartz tube furnace (QTF) and table top RTA system (RTP) as well as using conventional IR conveyor belt furnace (CBF).

There is a wide range of research activities worldwide that have exhibited the improved efficiency potential of crystalline silicon cells. Several researchers have attempted to study the effect of emitter diffusion contact formation on the performance of the screen-printed crystalline silicon solar cell. For example, Komatsu et al, have demonstrated that Manipulation of the doping profile of phosphorus emitters in silicon solar cells is an industry-applicable process. By changing the diffusion temperature-time curve without increasing process time, the surface phosphorus concentration has been reduced resulting in an efficiency gain of 0.2% absolute [18]. Shanmugam et al, have investigated the electrical and microstructural properties of screen-printed contacts formed with two different Ag pastes on phosphorus diffused silicon emitters with different surface doping concentrations and emitter depths. Low-resistance ohmic contact was demonstrated for phosphorus emitters with a surface doping concentration as low as  $1.7 \times 10^{20}$  atoms/cm<sup>3</sup>. The best PV efficiency (18.6%) was obtained for an intermediate surface dopant concentration of  $2.8 \times 10^{20}$  atoms/cm<sup>3</sup> [19]. Szlufcik et al, have concluded that for the cells with a non-selective emitter the phosphorus surface concentration should be at least  $10^{20}$ cm<sup>-3</sup>. Moreover, given the characteristics of screen-printed metal contacts, the junction depth should be at least 0.3–0.4  $\mu\text{m}$  so as to avoid shunting of the emitter achieved These constraints leads to maximum cell efficiency can be obtained. Small deviations from the optimum emitter profile result in drastic changes in cell efficiency [3]. Bottari et al have reported that the Rapid firing of screen-printed metallization is a critical step in the manufacture of crystalline silicon solar cells. Improved cell results are obtained with rapid heat-up and cool down, and they suggest that improved back contacts might be achieved with longer duration and slower cool temperature profiles [20]. Cooper et al have fabricated Si solar cells with the highly doping emitter and lightly doped emitters and using a range of peak firing temperatures. They find that as the emitter surface phosphorus concentration decreases, lower dark saturation current and higher final  $V_{\text{OC}}$  are observed; however, higher peak firing temperature is required to achieve low Ag/c-Si contact resistance and high FF [21]. Leong, 2013, have proposed improved the emitter formation by added new process to  $\text{POCl}_3$  diffusion process which is in-situ oxide film passivation process, this process eliminates the need to etch oxide film in dilute HF solution, it passivated the emitter layer, and it serves as the anti-reflection film, Taken together, these steps eliminate wet-chemical step, eliminate the need for anti-reflection film, and enhance manufacturing process throughput [22].

In this paper, the fabrication process simplification and cost-effective in parallel with the efficiency improvement of crystalline silicon solar cells has been evaluated. This has been by reducing and combined process steps as follows: (i) cleaning and saw damage etching combined in one processing step. (ii) (B2B) phosphorous diffusion process and designed as the in-situ oxide layer passivation process to avoid wet chemical step, eliminate the need for anti-reflection layer,

and enhance manufacturing process. As, a comparative study of the performance of mono-crystalline silicon solar cells with different drive-in diffusion temperatures have been investigated through investigate the effect of different temperature phosphorus diffusion on the conversion efficiency of the solar cells. The effect of peak firing temperature of three firing systems on the electrical performance of solar cell was investigated.

## 2. Experimental Procedure

In this study, 10x10 cm<sup>2</sup>, 200- $\mu$ m thick, <100> oriented, p-type Mono-crystalline (mc) Si wafers with bulk resistivity in 0.5-3  $\Omega$ -cm range were used. The process started with a cleaning and saw damage removal by etching of the as-cut wafers combined in one step as potential replacements for time-consuming and expensive standard RCA clean in 10 % NaOH at 70°C for 10 min followed by DI water rinse and removal of native oxide in dilute HF solution to form hydrophobic surfaces. The wafers were alkaline textured in KOH/IPA texturing process to create random pyramid features to reduce reflection as well as enhance light absorption followed by cleaning by HCl:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O solution at (1:1:6) solution at 70°C for 10 minutes. Moreover, the optimized the emitter formation process by use in-situ oxide film passivation during B2B POCl<sub>3</sub> diffusion process in the fabrication to form n<sup>+</sup> emitter layer by use tube furnace. To investigate the effect of different emitter sheet resistance ( $R_{sh}$ ) on the performance of the cell, we applied the process for different temperature and time, resulting in Emitter 1 (40 $\Omega/\square$ ), Emitter 2 (34 $\Omega/\square$ ), Emitter 3 (20 $\Omega/\square$ ), and Emitter 4 (14 $\Omega/\square$ ), respectively. After the diffusion process, Metallization was performed by screen printing with a commercially available Ag & Al pastes to form front contact and back surface field respectively. Screen-printed wafers were dried in a thermal oven for 10 minutes at 150°C. All Cells were then co-fired in industrial RTA 6-zone, conveyor belt furnace except some of cells with Emitter4 co-fired in the new firing systems: QTF and RTP. The set points for the 6-zone furnace have been summarized in table 1. Temperatures five temperature zones were kept fixed and only zone-4 temperature was varied from 800°C to 900°C at 20°C increments; the belt speed was kept constant at 75 inch per minute. While, the set point for the QTF and RTP have been summarized in tables 2 and 3, respectively. Finally, all the cells were edge isolated and tested.

Table 1. Conveyor Belt RTA Temperature Variation

No.	Zone 1(°C)	Zone 2(°C)	Zone 3(°C)	Zone 4(°C)	Zone 5(°C)	Zone 6(°C)
1	600	700	750	800	800	700
2				820		
3				840		
4				860		
5				880		
6				900		

Table 2. Three Zone Furnace Temperature Variation

No.	Zone 1(°C)	Zone 2(°C)	Zone 3(°C)	Peak firing temperature time (sec)
1	600	600	900	5
2			925	5
3			925	0

Table 3. Table Top System Temperature Variation

No.	Set temperatures	
1	RT-200°C (20sec)-400°C (20sec)-600°C (20sec)	780°C (1sec)
2	RT-200°C (30sec)-300°C (30sec)-400°C (30sec)	780°C (1sec)
3	RT-200°C (30sec)-300°C (30sec)-400°C (30sec)	780°C (1sec)

### 3. Results and Discussion

#### 3.1 Best Solar cell Characteristic

The I-V responses for the highest efficiency Si solar cell prepared with combined the Surface cleaning and saw damage removal steps in one step, B2B POCl<sub>3</sub> diffusion, and in-situ SiO<sub>2</sub> passivation/AR film are plotted in figure 1. The measurements reveal that used these simple and low-cost methods leads to the highest efficiency with V<sub>oc</sub>= 0.590V, J<sub>sc</sub>=29.7mA/cm<sup>2</sup>, FF=73 %, and efficiency= 12.8 %.

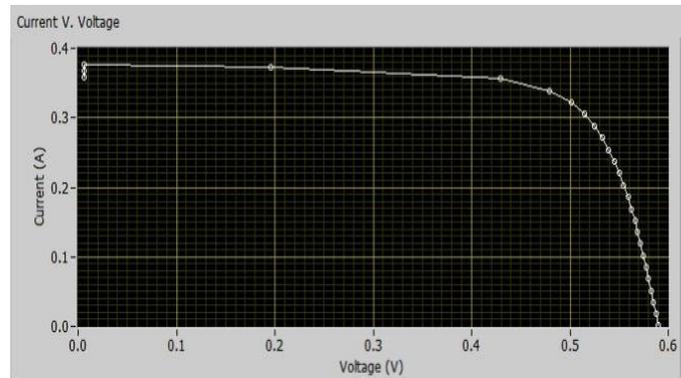


Fig. 1 the view of best I-V characteristic obtained.

#### 3.2 Analysis of Surface Texturing

The reflectance (R) of normal incident light on the silicon surface is determined by the complex refractive index  $n_c = (n - ik)$  of silicon and air:

$$R = \frac{(n_{c(Si)} - n_{c(air)})^2}{(n_{c(Si)} + n_{c(air)})^2} \quad (1)$$

Fig. 2(a) shows the wavelength dependence of the calculated front surface silicon reflectance from equation 1. The values of n and k for silicon at 300 K have been obtained from [23]. According to the data in figure 2(a) and the solar spectrum (AM1.5), it can be calculated that more than 30 % of solar light in the range of 400 to 1100 nm, which could participate to photo-generated current, is lost by front reflection. Surface texturing is an important process for silicon solar cells. By this process, pyramid structure can be formed on a silicon surface. The pyramid structure can make surface reflectance reduced, thus the loss of light can be declined and short current density can be improved.

Fig. 2(b) shows the measured reflectance curve for POCl<sub>3</sub> emitter-based screen printed mc-Si solar cell with in-situ oxide as passivation/ARC layer texturing by alkaline solution and PECVD SiN as passivation/ARC film based-solar cell as a reference cell. From the figure, it is noticed that in comparison with a reflectance curve of bare silicon the textured surface with in-situ oxide passivated/ARC layer exhibited significantly reduced in the reflection from 30% to 4-7%. In comparison with a SiN cell, the results show that the averaged SiN reflectance is 0.5 times lower than in-situ SiO<sub>2</sub>.

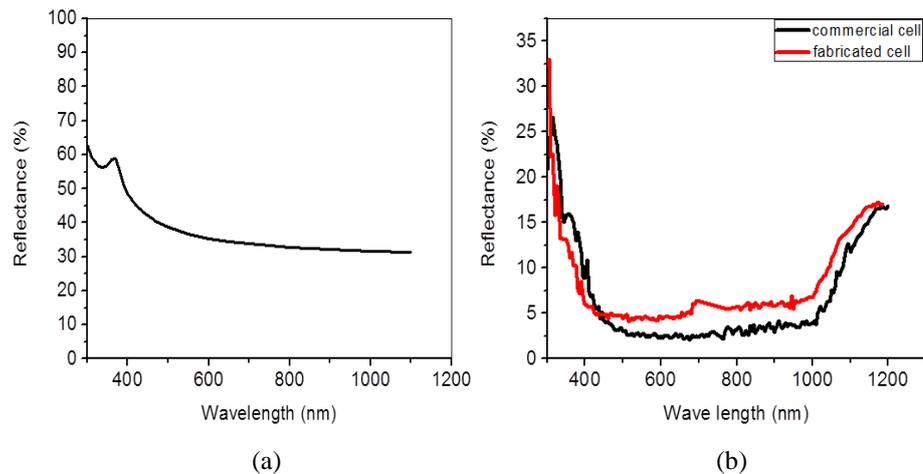


Fig. 2 (a) the Reflectance curve of bare Silicon (b) comparison of the reflectance curve of a fabricated cell and commercial cell

### 3.3 Analysis of Emitter Formation

The emitter sheet resistance can greatly influence the solar cell characteristics such as junction shunting, contact resistance, open-circuit voltage, and short wavelength response. Decreasing the phosphorus surface doping concentration leads to a higher contact resistivity. The diffusivity of phosphorus ( $D_p$ ) at the phosphorus concentration ( $P_c$ ) of  $1 \times 10^{20}$  atoms/cm<sup>3</sup> lower than the ( $D_p$ ) at ( $P_c$ ) of  $1 \times 10^{19}$  atoms/cm<sup>3</sup> [24]. This causes the formation if possible to say two different layers with different ( $P_c$ ), which are called very heavy doped layer and heavy doped layers. The one of a positive effect of the existence of the very heavy doped layer is that it enables a good contact with silver print paste with relatively low resistance. One of the negative effects is that the very heavily doped phosphorus results in an increased carrier recombination [25]. The heavy doped layer needed to be relatively deeper with lower doping. Therefore, the direction of improving industrial emitters should be toward a shallower very heavy doped layer to minimize carrier recombination, which can be achieved by reducing diffusion time [18], and a deeper heavy doped layer to compensate for the loss in lateral conductivity in the very heavy layer.

Figure 3 plots the electrical performance of the screen printed mc-Si solar cells processed using Emitter 1, Emitter 2, Emitter 3, and Emitter 4 at firing temperatures 820°C. Each point represents an average of six values. From the figure, it can be observed that the batch top efficiency for Emitter 2 increased by 2.5% absolute compared to the second top efficiency which recorded for emitter 3 solar cells. The main contribution for efficiency improvement occurs from the gain in  $J_{sc}$ , which increased by 3.1 mA/cm<sup>2</sup>, and the gain in  $V_{oc}$  which increased by 11 mV for the Emitter 2 which may be caused by both low surface ( $P_c$ ) and shallow very heavy doped layer. We think that the big difference in FF and  $J_{sc}$  between the Emitter 2 and the rest of the Emitters attributed to shallow very heavy doped layer when contact with silver metal. My opinion that the manipulated the doping profile in simple ways result in efficiency improvement.

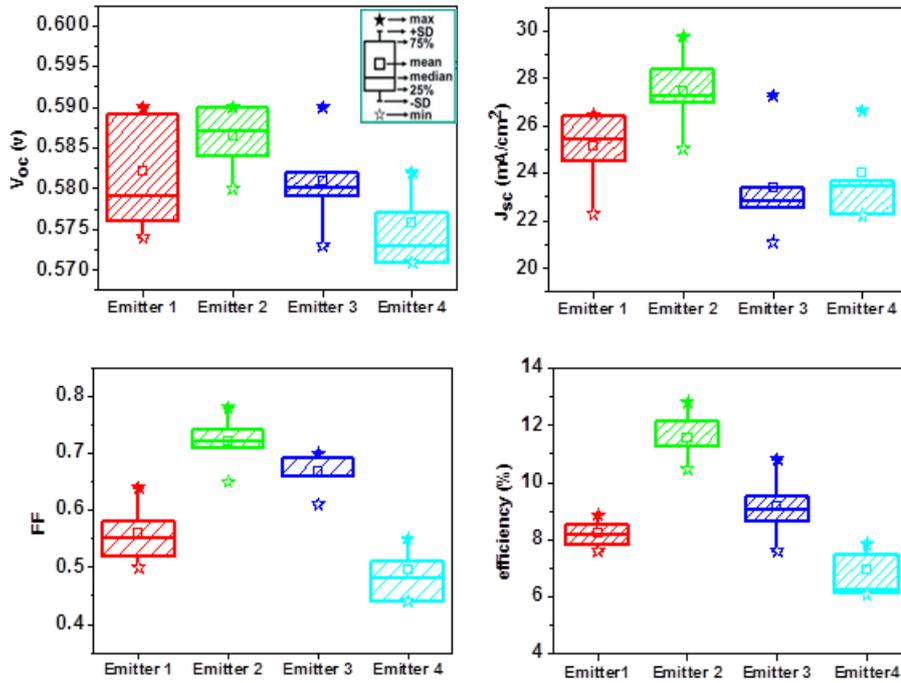
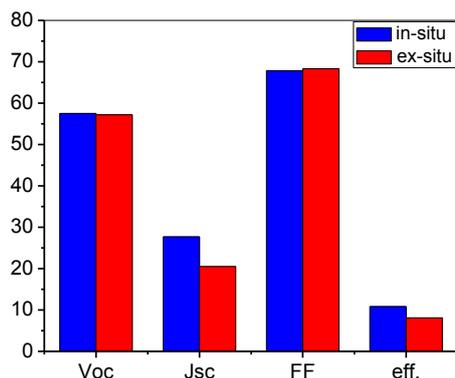


Fig. 3 Emitters dependence of the electrical performance of the  $POCl_3$  emitter-based screen printed mc-Si solar cell with in-situ oxide

### 3.4 Analysis of Surface Passivation

Fig. 4 shows the comparison of average values of ( $V_{oc}$ ), ( $J_{sc}$ ), (FF), and efficiency for the emitter 2 of solar cell passivated with in-situ oxide layer and solar cell passivated with a thermal oxide layer at all firing temperature. experimentally, all the experimental procedures in this section event simultaneous with experimental procedures in the section 2 except that after the diffusion process, HF dip to remove the phosphosilicate glasses and in-situ oxide and the wafers were then deposited a narrow, passivated films by performing thermal oxidation at 1000°C for 40 min in  $O_2$  atmosphere. From the figure, it can be noted that the average value of efficiency of solar cell passivated with in-situ oxide layer higher than solar cell passivated with a thermal oxide layer. The increase in efficiency for cell coated by in-situ oxide is supported by an appreciable increase in current density due to cancellation the high temperature treatment during the thermal oxide growth. These can severely degrade the bulk carrier lifetime and therefore reduce the current density.

The current density between the solar cell with ex-situ oxide and solar cell coated with in situ oxide is increased from 20.5mA/cm<sup>2</sup> to 27.7mA/cm<sup>2</sup>, which is a 35% increase. For open circuit voltage, there is slightly increment which is from 0.572 V to 0.575 V and taken accounted for 0.5 % increase. While the average values of FF are very close to both cells due to that the fill factor is insusceptible by the surface passivation. The overall efficiency of solar cell with thermal oxide compared with solar cell coated with in situ oxide is 8.1 % to 10.8%, which is an increase of 33%. Therefore, there is significant improvement in efficiency of solar cell passivated with in-situ oxide layer.



*Fig. 4 comparison of average values of ( $V_{oc}$ ), ( $J_{sc}$ ), ( $FF$ ), and ( $eff.$ ) for the emitter 2 of solar cell passivated with in-situ oxide layer (dark colour) and solar cell passivated with a thermal oxide layer (light colour) at all firing temperature.*

### 3.5 Analysis of Contact Formation

For screen-printed solar cells, the peak firing temperature in the firing process is extremely important to the performance of the solar cells. Studies by Shiliang Wu et al [26] and Kwon et al [13] have reported a direct correlation between peak temperature and cell efficiency. Under firing results in an insufficient dielectric opening, while over firing leads to the top contact shunts directly to the base [27, 28]. Figure 5 plots the variation of I-V characteristics ( $FF$ ,  $Eff$ ,  $V_{oc}$ , and  $J_{sc}$ ) with peak firing temperature in emitter 2 configuration. Each point represents an average of six values. The maximum averaged open circuit voltage was 0.585 V at peak firing temperature 800 °C. The maximum averaged short-circuit current density was 28.1mA/cm<sup>2</sup> at peak firing temperature 800 °C. As peak firing temperature increases, average values of efficiency,  $V_{oc}$ ,  $J_{sc}$ , and  $FF$  decrease linearly; 820 °C appears to be the optimum annealing temperature. Figure 6 plots solar cell series and shunt resistances as a function of peak firing temperature. As a function of temperature, series resistance appears to increase slightly over a broad temperature with a rapid rise at ~ 880 °C while the shunt resistance decreases with temperature. The shunt resistance decreases with temperature.

Moreover, this firing process is also important to back side metallization using screen printing. After firing process on back side metallization, back surface field (BSF) is formed between crystalline silicon wafer and Al back contact. The BSF is highly Al doped Si layer, and the layer acts as a p+ layer. This p-p+ region form an electric field and create a barrier to minority carrier flow to rear side. The BSF layer thus has an effect that minimizes the rear surface recombination velocity. When the peak Al-Si alloying temperature exceeds a critical value, Al surface reveals a lot of bumps and BSF layer becomes non-uniform.  $V_{oc}$  of solar cells is affected by uniformity of BSF layer thus decline electrical performance of solar cells [29].

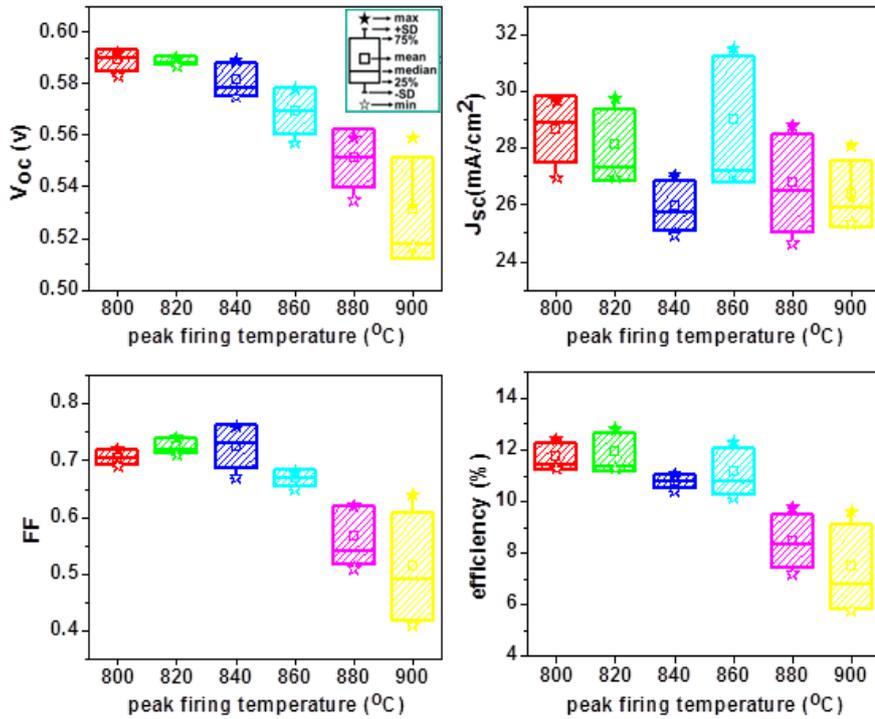


Fig. 5 peak firing temperature dependence of the electrical performance of the  $POCl_3$  emitter-based screen printed mc-Si solar cell for Emitter 2 with in-situ oxide

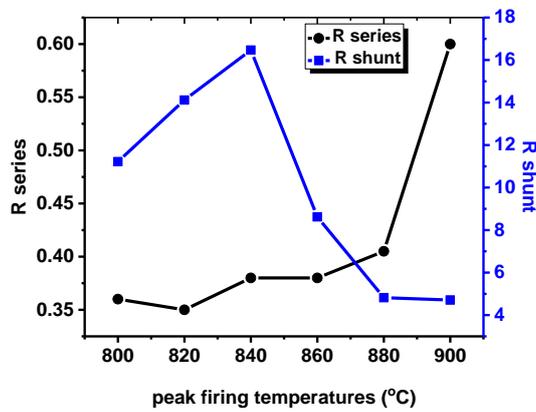


Fig. 6 shown the change of series and shunt resistance with peak firing temperatures

Therefore, at higher temperature (880°C and 900°C), agglomeration or bumps was occurred and disturbed uniform BSF layer formation as well as increase the back side recombination velocity (BSRV). Figure 7 shows the internal quantum efficiency (IQE) at long wavelength for two screen-printed silicon solar cell with emitter 2 fired at 800°C and 900°C, the results confirm that fired at high peak firing temperature causes increase BSRV.

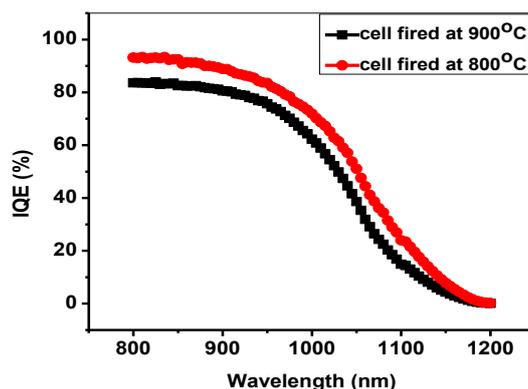


Fig. 7 long wavelength internal quantum efficiency (IQE) for two screen-printed silicon solar cell with emitter 2 fired at 800°C and 900°C

Among the efforts to the fabrication process simplification and cost-effective in parallel with the efficiency improvement of crystalline silicon solar cells, firing of screen-printed contacts using QTF and RTP is a promising alternative compared to infrared heated conveyor belt furnaces due to its requirement of less process time and thermal budget. The crucial step in the use of any heating system for firing process is temperature profile specifically a novel heating configuration. The best temperature profile was obtained in both QTF and RTP shown in table 3 and table 4 respectively. All the solar cells fired by QTF and RTP are screen printed mc-Si solar cell with emitter 4. The distribution of performance parameters of the fired cells by QTF is shown in table 4. The cell fired by temperature profile no.1 shows the best combination of performance parameters with 580 mV, 22.7mA/cm<sup>2</sup>, 0.719 and 9.4% as the corresponding values of  $V_{oc}$ ,  $J_{sc}$ , FF, and efficiency, respectively. While, the distribution of performance parameters of the fired cells by RTP is shown in table 5. The cell fired by temperature profile no.2 shows the best combination of performance parameters with 581 mV, 25mA/cm<sup>2</sup>, 0.729 and 10.5% as the corresponding values of  $V_{oc}$ ,  $J_{sc}$ , FF, and efficiency, respectively.

Table 4.  $V_{oc}$ ,  $J_{sc}$ , FF, and efficiency of solar cell with emitter4 fired by QTF

No. of temperature profile	$V_{oc}$ (v)	$J_{sc}$ (mA/cm <sup>2</sup> )	FF	eff. (%)
1	0.580	22.744	0.719	9.4
2	0.563	20.216	0.664	7.5
3	0.561	21.744	0.525	6.4

Table 5.  $V_{oc}$ ,  $J_{sc}$ , FF, and efficiency of solar cell with emitter4 fired by RTP

No. of temperature profile	$V_{oc}$ (v)	$J_{sc}$ (mA/cm <sup>2</sup> )	FF	eff. (%)
1	0.572	20.352	0.718	8.3
2	0.581	25.016	0.729	10.5
3	0.567	21.96	0.711	8.8

Fig. 8 shows the best I-V curve for the solar cell with emitter 4 fired by CBF, QTF, and RTP. The results indicate that the solar cell fired by RTP has a highest efficiency compared with CBF and QTF. While, the I-V curves of the solar fired by QTF and CBF are almost identical.

Therefore, both QTF and RTP systems offer a highly attractive low-cost alternative to expensive and high thermal budget industrial conveyor RTA furnaces.

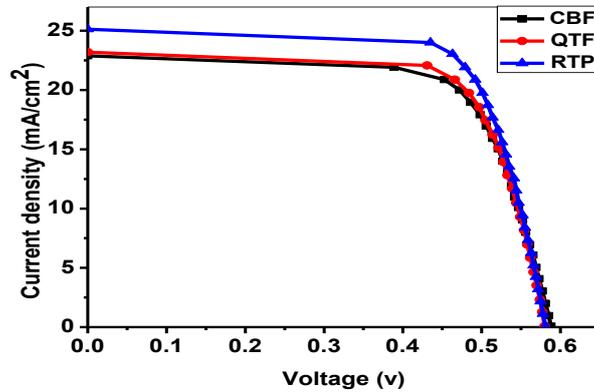


Fig 8. the best I-V curve for the solar cell with emitter 4 fired by CBF, QTF, and RTP

Fig. 9 shows the five curves of IQE for  $\text{POCl}_3$  emitter based-screen printed Si solar cell with four different efficiencies as well as a reference cell. As see, the IQE data is in very good agreement with the electrical parameters of the four cells where cell4 shows best IQE curve with higher efficiency. From the figure, at the blue or short wavelength region, the cell4 exhibits higher IQE than the cell3 which in turn is higher than cell2, and rear word cell1. This indicating that the cell4 have best surface passivation and lowest surface recombination velocity. At the medium wavelength, the cell3 shown a little precedence over the cell4 this may be indicating that cell3 have the best junction. At the red or long wavelength region, it can be observed that there is the sizable agreement between IQE of a reference cell and cell4 and cell3 at the wavelength is 800nm. Also after 1000nm there is convergence in IQE data and this is confirmed by the identical values of  $V_{oc}$ .

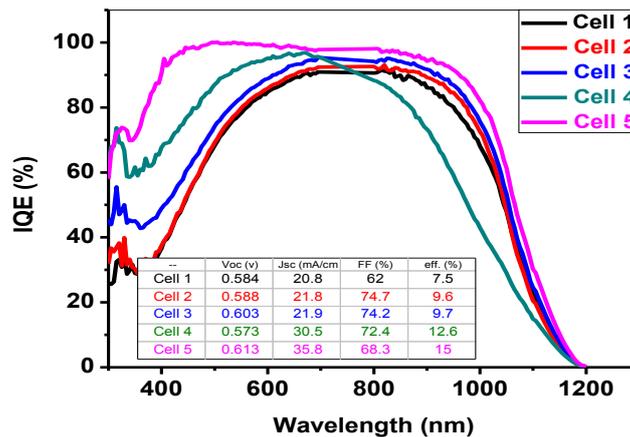


Fig. 9 the IQE of four different  $\text{POCl}_3$  emitter based-screen printed mono-c Si solar cell as well as reference cell

#### 4. Conclusions

A simplified approach for high-efficiency silicon solar cell processing is introduced in an attempt to reduce the cost of the solar cells. The procedure introduces three main features. First, Surface cleaning and saw damage removal combined in one step to overcome on the risky and

time consuming in the conventional cleaning approach. Second, simplifying the diffusion process by using Back to back diffusion with reference 22 diffusion method this leads to eliminate wet-chemical step, eliminate the need for anti-reflection film, and enhance manufacturing process throughput. Third, Firing of screen-printed solar cells using QTF and RTP as a promising alternative compared to infrared heated conveyor belt furnaces due to its requirement of less process time and thermal budget. Moreover, we investigated the electrical properties of screen-printed mono-crystalline Silicon solar cells formed with four different phosphorus diffused silicon emitters and different peak firing temperature of three firing systems on the cells performance were investigated.

The best conversion efficiency ~13% was obtained for the Emitter 2 cell fired by CBF, with a  $V_{oc}$  of 590mV,  $J_{sc}$  of 29.7mA/cm<sup>2</sup>, and FF of 73%, which are the largest among the four Emitters. While, the emitter 4 based-screen-printed solar cells fired by QTF produced a cell efficiency of 9.4% with  $V_{oc}$  of 580 mV,  $J_{sc}$  of 22.7 mA/cm<sup>2</sup>, and FF of 0.719. as for, the emitter 4 based-screen-printed solar cells fired by RTP produced a cell efficiency of 10.5% with  $V_{oc}$  of 581mV,  $J_{sc}$  of 25 mA/cm<sup>2</sup>, and FF of 0.729. these results superior to the measured values for emitter 4 based-screen-printed solar cells fired by CBF which made a cell efficiency of 7.1% with  $V_{oc}$  of 573 mV,  $J_{sc}$  of 24.1 mA/cm<sup>2</sup>, and FF of 0.513. This implies these less process time and thermal budget heating configurations system is a promising alternative compared to CBF.

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